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Volt-ampere characteristics of semiconductor pinch-off diodes prior to pinch-off

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**Iowa State University of Science and Technology
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VOLT-AMPERE CHARACTERISTICS OF SEMICONDUCTOR
PINCH-OFF DIODES PRIOR TO PINCH-OFF

by

Dale Wendell Bowen

A Dissertation Submitted to the
Graduate Faculty in Partial Fulfillment of
The Requirements for the Degree of
DOCTOR OF PHILOSOPHY

Major Subject: Electrical Engineering

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In Charge of Major Work

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Ames, Iowa

1963

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INTRODUCTION

Shockley (14) proposed a device known as a unipolar or field-effect transistor in 1952. This device deviates radically from the regular concept of a transistor in that it is a majority carrier device rather than a minority carrier device. It is a direct semiconductor analog of the vacuum tube. It exhibits extremely high input impedances and low output impedances as contrasted to the conventional transistor.

Figure 1 shows the device proposed by Shockley. It consists of a rectangular bar of semiconductor material with a square cross-sectional area. For various reasons the main body is chosen to be n-type semiconductor material. Around the entire body of the device is placed by some technique, diffusion or alloying, for example, a belt of p-type material.

For the configuration chosen, one end of the bar, the source, is grounded; the other end, the drain, is run at a potential positive with respect to the source. The gate is run negative with respect to the source.

Under these conditions the p-n junction formed by the gate p-type material is reverse biased. The doping levels are arranged to cause the depletion region to move into the n-type material. As the gate voltage is made more negative for a fixed drain voltage or as the drain is made more positive for a fixed gate voltage, the reverse bias increases on the p-n junction.

How the depletion region moves into the bar relative to the reverse bias voltage will be discussed later. It suffices to know at this time

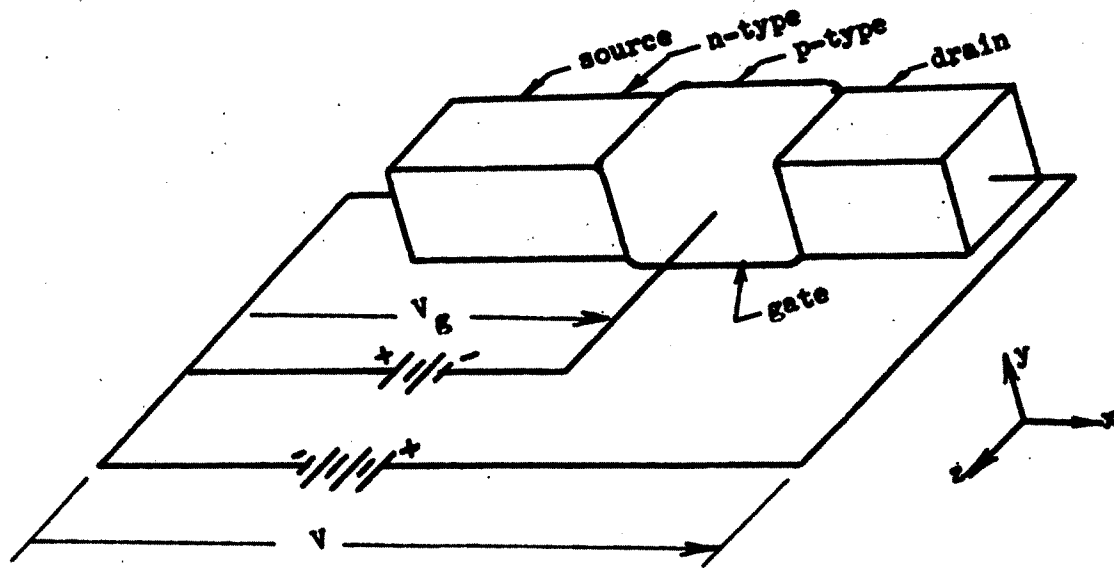


Figure 1. The Schockley field-effect transistor

that it does. The depletion region of a reverse biased p-n junction is virtually mobile charge free; hence, the depleted volumes in the bar are no longer available to conduct carriers from the source to the drain. The net effect is to modulate the conductivity of the bar.

For changes in reverse bias voltage, the current-voltage characteristic varies considerably from a linear relationship. It will be shown in detail in Appendix A that the current-voltage relationship for zero gate voltage is

$$I = \frac{a^2}{\rho L} \left[V - \frac{4}{3} \frac{V^2}{V_0} + \frac{1}{2} \frac{V^2}{V_0} \right] \quad (1)$$

In this equation a is the side dimension of the bar, L the length of the gate junction in the direction of current flow, ρ the bulk resistivity of the n-type material, V_0 a voltage called the pinch-off voltage, and V the drain voltage. The derivation of equation 1 requires that $L \gg a$ in order that integration may be utilized.

The reverse bias can be increased only so far until a saturation condition exists. As the reverse bias increases, the cross-section of the depleted area increases. When a certain voltage is reached, the cross-sectional area of the depleted region becomes the cross-sectional area of the n-material. This condition occurs first at the end of the p-n junction nearest the drain. The voltage at which this condition exists is called the pinch-off voltage, V_0 .

As reverse bias is further increased, the pinch-off condition travels from the drain end of the p-n junction toward the source. During this voltage condition, the current is more or less saturated. Generally the

current-voltage characteristic exhibits a small positive slope. This situation occurs because the effective length, L , of the gate junction decreases. Analytic solutions of this portion of the current-voltage characteristic are difficult.

After the total p-n junction region is pinched-off, further increase in reverse bias will eventually lead to breakdown. Current runaway results. Breakdown is caused by material considerations. Primarily it is a result of electric fields existing in the semiconductor which cause electron-hole multiplication (10).

Figure 2 shows one of a family of field-effect transistor current-voltage curves. The ordinate is current and the abscissa voltage normalized with respect to the pinch-off voltage V_0 . If all the curves were shown, a set of curves similar to a set of pentode plate characteristics would result. The free parameter would be the gate voltage.

Region I illustrates the diode current-voltage relationship below pinch-off. Region II describes the saturation condition where the pinch is travelling from the drain to the source. Region III describes the breakdown condition. Depending on material and geometrical considerations, the regions, especially II and III, may overlap.

If a field-effect transistor is operated in Region I, it may be thought of as a variable resistor. For the geometry discussed, equation 1 shows the current-voltage relationship. This equation comes from a particular geometry and material constitution. The question now arises. Is it possible to tailor-make a current-voltage characteristic? What factors influence the characteristic?

This dissertation will show what factors affect the current-voltage

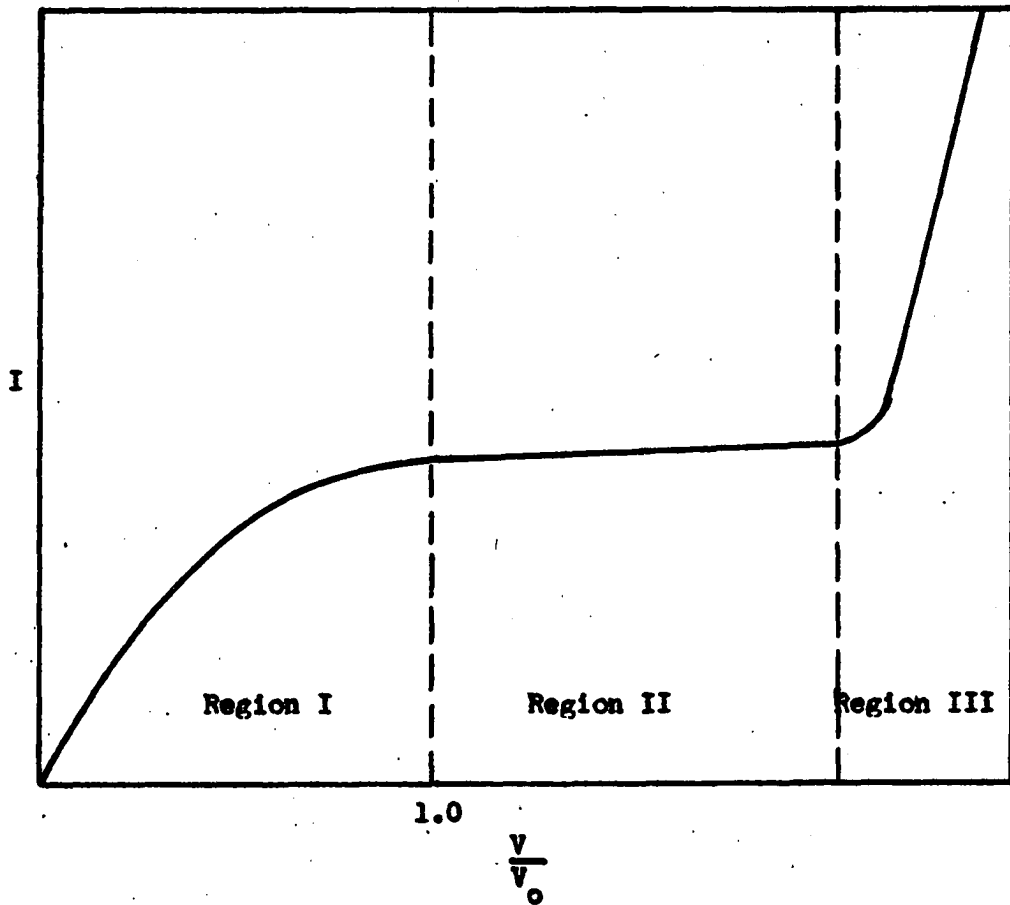


Figure 2. The current-voltage characteristic of a field-effect transistor for zero gate voltage

characteristic, both as to shape and as to current and voltage magnitude. In order to have some concrete current-voltage characteristic to design for, this dissertation will show that it is possible to tailor-make a current-voltage characteristic that obeys the equation

$$I = K V^{\frac{1}{2}} \quad (2)$$

K is a constant relating coefficient which will also be defined.

If one drives a device which obeys equation 2 with a current I, the device may be used as a square law detector. Square law detectors have several important uses, the most important being the measurement of power.

So far a field-effect transistor which is driven with zero gate voltage has been discussed. Zero gate voltage means the gate is grounded to the source. The field-effect transistor is a four terminal device. Since this investigation will consider only devices with gates and sources in common and driven in Region I, the four terminal device may just as well be considered a two terminal device. Rather than consider the device to be a field-effect transistor, one may consider the device as a special type of diode. This diode will be called a pinch-off diode.

The first pinch-off diode that will be considered is a rectangular bar with a rectangular cross-section. The device is shown in Figure 3. On the entire bottom side p-type material will be diffused, alloyed, or deposited onto the bulk n-type bar. On the p-type layer a conducting layer will be coated and continued to the source end. This layer will insure a good ground between the gate junction and the source.

Shockley chose a device which had a long x-dimension relative to its

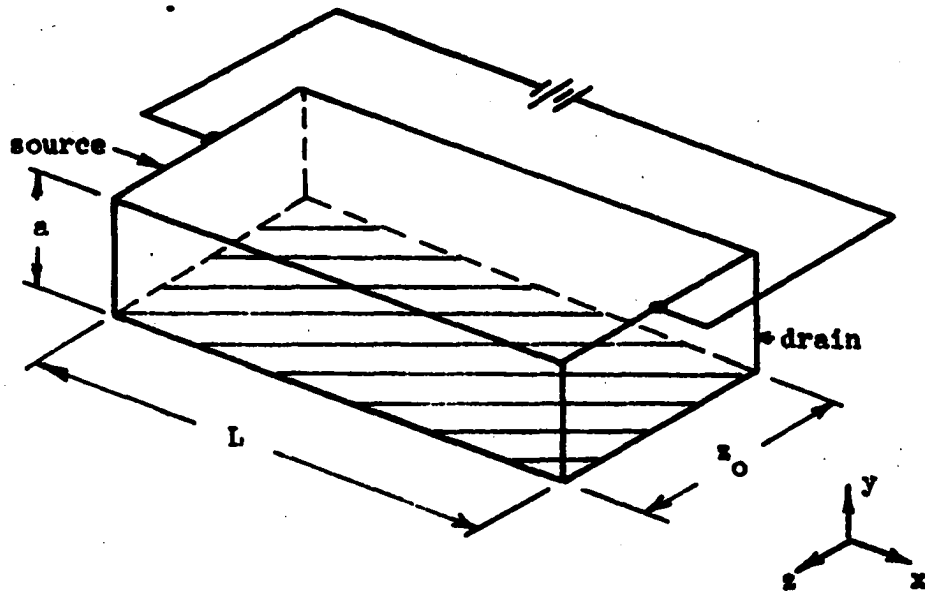


Figure 3. Rectangular bar pinch-off diode

y-dimension. This condition insures that the constant potential areas in the y-z plane will be perpendicular to the x axis. Under this condition, a one-dimensional integration of Ohm's law in differential form may be accomplished for a few specific geometries, Shockley's example for one.

Whether these devices when fabricated will have large length to height ratios is subject to question. In all likelihood, they will not; consequently, it will not be permissible to attempt a one-dimensional integration of Ohm's law. It is possible a two-dimensional integration, assuming the devices proposed have uniform cross sections in the z-direction, could be effected; however, the two-dimensional integration may become difficult.

It will be shown later that the depletion layer depth along the x-direction will vary with the square of the voltage existing along the diode in the x-direction. The voltage existing along the bar in the x-direction is dependent on the configuration of the conducting volume of the diode. The depletion layer depth and voltage distribution interact. In all but a few special geometries, the interaction is not clear when the height to length ratio is small.

The fact that the height to length ratio will be small and the depletion layer depth-voltage distribution uncertainty mitigate against using integral techniques for determining the current-voltage relationships prior to pinch-off. Another technique will be employed to determine the current-voltage relationships. This method involves computing the resistance of the diode for various applied voltages below pinch-off. The resistance will be determined by means of curvilinear square techniques. Once the resistance for a given voltage is known, the current may be computed. From

this point by point solution, the current-voltage characteristic for a particular geometry may be determined.

Starting with solution for the geometry of Figure 3, it will be shown that the desired current-voltage relationships may be generated through an iterative process. The geometry will be adjusted slightly. A new current-voltage curve will be formed. From the new one, further geometrical adjustments will be made until the relation of equation 2 is achieved.

BACKGROUND MATERIAL

P-n Junction Depletion Layer Depth-Voltage Relation

The voltage existing across the negatively biased gate diode junction is governed by Poisson's equation provided that the charges in this depletion region are primarily fixed in the lattice sites and not mobile. The charges result from the impurities introduced into the crystal during its manufacture. No mobile charges exist in the depletion region since the electric field, E , is of such polarity to sweep them out of the depletion region.

Poisson's equation in one-dimension may be stated as

$$\frac{\partial^2 V}{\partial y^2} = - \frac{\rho}{\epsilon} \quad (3)$$

where V is the voltage, y the dimension in the y -direction, ρ the charge density at the particular location and ϵ the permittivity of the semiconductor material. Of course a consistent set of units must be employed. A one-dimensional Poisson's equation will be solved since the geometries to be investigated will be proposed to have a one-dimensional depletion region penetration.

The p-n junction to be discussed is shown in Figure 4. This junction is known as a step junction since it rapidly changes from p-type material to n-type material. Various fabrication methods exist (3,9). Other types of junctions such as the graded junction exist.

The physical boundaries of the p-type material are at y -dimensions of d and zero. The distance d is negative. The physical boundaries of the

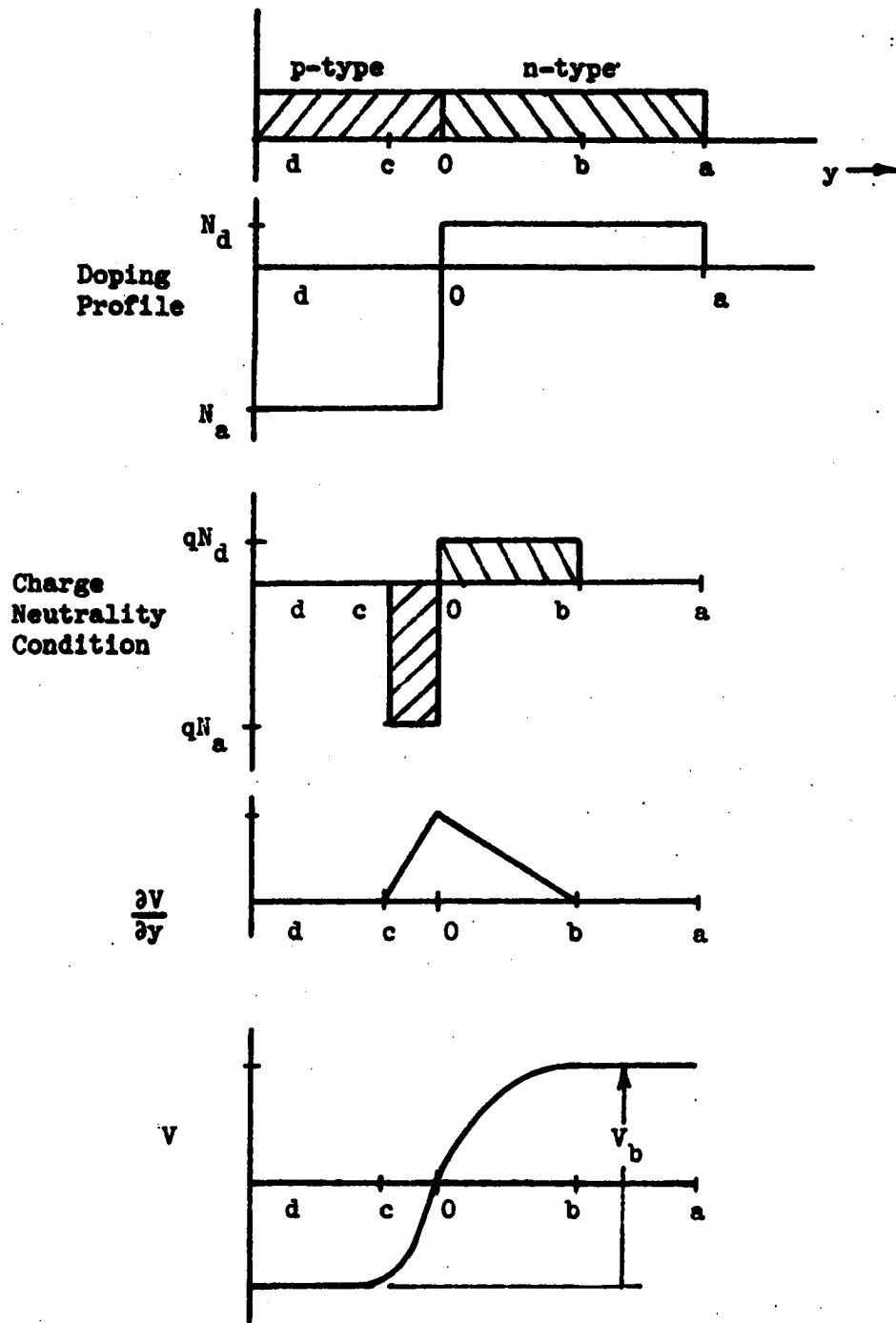


Figure 4. The doping profile, $\frac{\partial V}{\partial y}$, and V of a step p-n junction

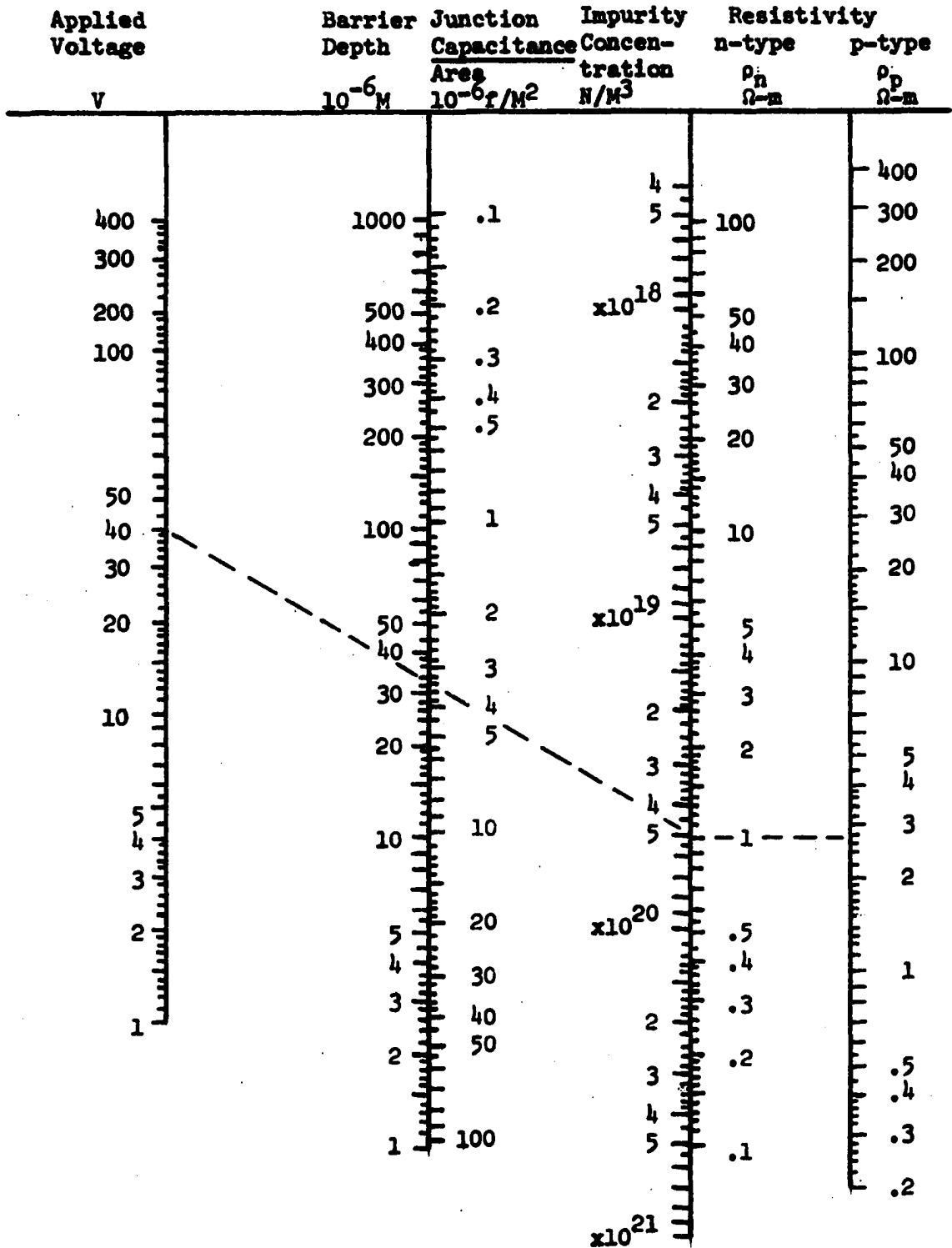


Figure 5. Nomograph for a silicon diode with a step junction

impurity concentration. This equation assumes $N_d \gg N_a$. A similar equation for $N_a \gg N_d$ could be readily developed and would plot similarly.

The relationship between the impurity concentration and the resistivities comes from

$$\rho = \frac{1}{q(n \mu_n + p \mu_p)} \quad (14)$$

where ρ is now the resistivity of the material which becomes depleted, n the concentration of negative charges, p the concentration of holes, μ_n the electron mobility and μ_p the hole mobility. For silicon μ_n is 0.12 meter² per volt-second, and μ_p is 0.045 meter² per volt-second.

For the n-type material in the extrinsic region, as is the case being considered, equation 14 becomes

$$\rho_n = \frac{1}{q \mu_n N_d} \quad (15)$$

where ρ_n is the resistivity of n-type material. Mattson (12) discusses the concentration-resistivity relationship for semiconductor materials in some detail. The relationship between ρ_n and N_d is plotted in Figure 5. A similar relationship could be developed for p-type material. The result is plotted on the figure as the right-hand column.

Resistance Determination by Curvilinear Squares

One may determine the resistance presented by the material between the two cross-hatched areas in Figure 6 by applying equation 16 provided certain conditions are obeyed.

$$R = \int_0^L \frac{\rho dx}{A} \quad (16)$$

in comparison to n-type will be applied. This statement means that $N_a \gg N_d$.

If N_a is greater than N_d by a factor of a thousand or more, the inequality condition is readily met. During diffusion of impurities, alloying or vapor depositing of p-type materials, this condition can readily be attained.

When the inequality is applied to equation 11 while noting equation 9, equation 11 becomes

$$V_b = \frac{q N_d}{2\epsilon} b^2 \quad (12)$$

This equation points out the fact that the applied voltage varies with the square of the depletion region depth.

When the voltage applied is of such magnitude that the depletion region reaches to the n-type boundary a , the pinch-off condition for the pinch-off diode exists. The pinch-off voltage, V_o , is then

$$V_o = \frac{q N_d}{2\epsilon} a^2 \quad (13)$$

Figure 5 shows a nomograph relating the applied voltage, depletion region depth, junction capacitance, impurity concentration, and n-type and p-type resistivity for a silicon diode with a step junction. More will be said about the junction capacitance in a later section.

Silicon is used as an example for the plot. A similar nomograph could be developed for germanium or any of the intermetallic compound semiconductors. Silicon is appealing because of the high resistivities available and its low reverse bias current characteristics.

Equation 12 relates the applied voltage to the barrier depth and

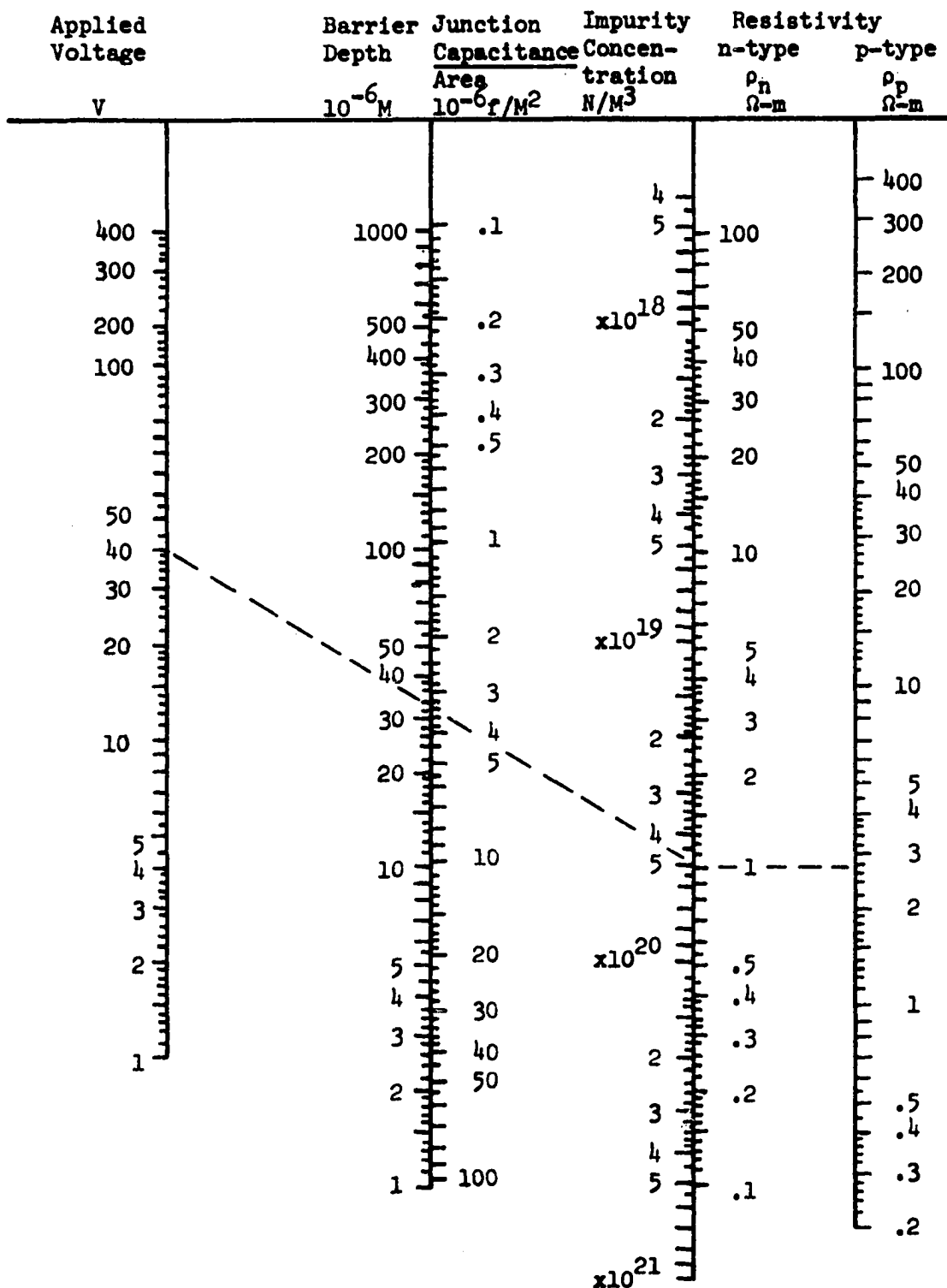


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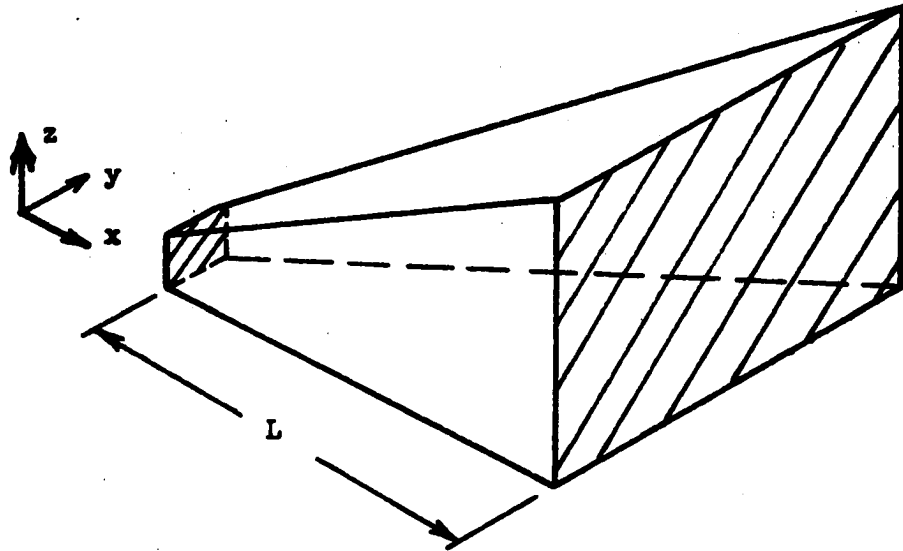


Figure 6. The geometrical configuration of a resistance

In this equation R is the resistance presented, ρ the resistivity in a consistent set of units, A the cross-sectional area perpendicular to the x -axis and L the length between faces.

If the resistivity varies with the x displacement, only the functional relationship need be known in order to effect a solution for the resistance. In the diode configurations to be considered, the resistivity will be a constant along all axes considered; consequently, ρ may be brought out to the left of the integral.

Strictly speaking, one may use equation 16 only when the cross-sectional area A is constant over the whole length L . Under this condition

$$R = \frac{\rho L}{A} . \quad (17)$$

The reason that A must be constant is to keep the constant potential surface and the cross-sectional area normal to the x -axis at any particular x value superimposed. This condition is necessary to keep the current flow lines normal to the constant potential surface--a condition which must always be obeyed. Since a one-dimensional integration is proposed, the current flow lines must be in line with the x -direction.

Reasonably accurate results for the resistance of Figure 6 may be obtained when A is not constant provided that any variation in the y - or z - direction is small compared to the dimension L . Typically, if a height or width variation can be restricted to one-tenth the dimension L , errors in computed resistance will be small. Of course the functional relationships of the y - and z - dimensions in terms of the x -direction must be known.

To further simplify the diode configuration, the z-dimension will be fixed at a value z_0 , and the y-dimension will be allowed to vary in various manners. Under these restrictions, equation 16 becomes

$$R = \frac{\rho}{z_0} \int_0^L \frac{dx}{y} \quad (18)$$

where $y = g(x)$.

How does one determine the resistance of a configuration in which the y-dimension variation is appreciable compared to the dimension L? Generally, integration is abandoned and the method of curvilinear squares adopted when the problem is two-dimensional. If the problem were three-dimensional, curvilinear cubes could be investigated.

Essentially one must know where the constant voltage lines and current flow lines are in the x-y plane. How these may be systematically determined will be discussed in the next section. The only comment that need be advanced now is that the current flow lines are always orthogonal to the constant potential lines.

Consider the curvilinear rectangle of Figure 7. Assume that the distance between the two arbitrarily chosen constant voltage lines, V_1 and V_2 , is l -units. Two current flow lines are drawn which intersect the voltage lines at right angles. The spacing is chosen to be the distance p .

The resistance of the volume associated with the curvilinear rectangle is

$$R = \frac{\rho}{z_0} \frac{l}{p} \quad (19)$$

If the potential spacing and current flow line spacing are chosen such that $l=p$, the rectangle becomes a square; and the resistance presented is

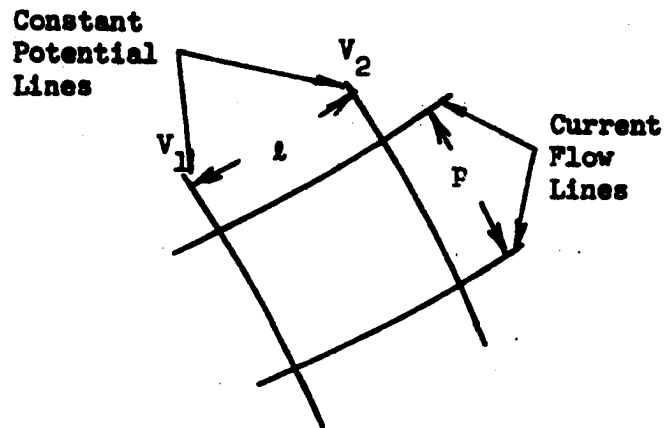


Figure 7. A curvilinear square

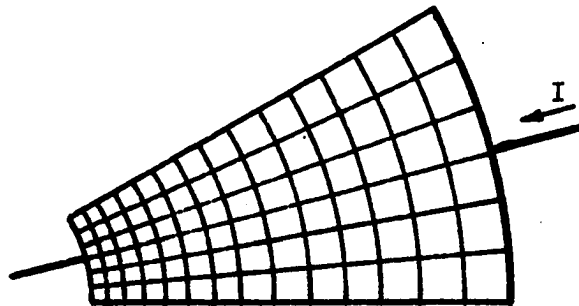


Figure 8. A curvilinear square determination of the resistance of a resistor

independent of the distances l and p .

$$R = \frac{\rho}{z_0} \quad . \quad (20)$$

Suppose that a device, which has a y -dimension variation appreciable with respect to its length, is divided into curvilinear squares as shown in Figure 8. There are n squares in the direction of current flow and s squares in the direction of the constant voltage lines. The n resistance squares effectively add in series; whereas, the s resistance squares combine as if in parallel. The total resistance presented by the device is thus

$$R = \frac{\rho}{z_0} \frac{n}{s} \quad . \quad (21)$$

In Figure 8, $n = 14$ and $s = 6$. $R = \frac{14}{6} \frac{\rho}{z_0}$.

In order that the resistance may be expressed in ohms the resistivity and z_0 must have consistent dimensions. As long as n and s are of the same units, what they are is not important.

There are several ways to arrive at the curvilinear squares of Figure 8. A particular geometry may point toward a particular method of generating the squares. Boast (4,5) and Bewley (1) point out various methods.

Finite-difference Equation Solution to Laplace's Equation

The boundaries of the curvilinear squares are either equipotential lines or current flow lines. Since the current flow lines are orthogonal to the equipotential lines, one need know only the potential distribution in the conducting region of the diode in order to determine the resistance

of the diode for any particular configuration at any particular applied voltage.

There are several methods to effect a solution for a given configuration. One is just by trial and error. By incorporating the fact that the potential function is normal to the non-terminal boundaries along with the potential-current orthogonality conditions, one may effect a solution. Since many geometrical configurations are to be considered and various voltage levels for each configuration investigated, trial and error procedures involve too much non-rewarding effort.

Another possibility is to find certain transform pairs which will convert the proposed geometrical figures into configurations for which the potential distribution is known or is readily obtainable. The configurations are roughly trapezoidal. The Schwarz-Christoffel transformation (8), a useful tool for investigating degenerate polygons, could probably be used for the solution; however, it appears some of the integrations would be graphical and that a third possible method would be easier.

The third method takes advantage of the fact that the potential distribution in the conducting portion of the diode obeys Laplace's equation. By using the condition that the non-terminal boundaries are current flow lines and thus the equipotential lines are normal to them, one may use these boundary conditions and Laplace's equation to obtain the potential distribution. Boast (6) describes methods to solve Laplace's equation by means of finite-difference equations.

The multitude of equations that is generated by a solution by finite-difference equations lends itself to a computer solution. Since the configurations vary slightly from voltage level to voltage level and,

once a grid point pattern is set, geometrical variations are easily accomplished, this method is the one that will be implemented.

A solution of Laplace's equation by finite-difference equations involves setting up a two-dimensional array of potential points within the boundaries of the conductor. By looking at the potentials of the nearest neighbor of any specific point, one may speculate about the potential, first derivative, and second derivative of the specific point. Actually a more general solution involving the three dimensional Cartesian coordinate system, cylindrical coordinates, or spherical coordinates may be developed. Since the geometries involved will be uniform in one dimension, the z-dimension, a two dimensional solution will be developed in the x-y plane.

In order to develop an expression for the first derivative of the potential function, $V_{x,y}$, with respect to the x-coordinate, one must look at the potential of the grid points to the right and left of $V_{x,y}$. These points are at Δx distance to the right and left and are labeled $V_{x+\Delta x,y}$ and $V_{x-\Delta x,y}$.

Figure 9 shows a plot of V with respect to the x-dimension. One may approximate the partial derivative of V with respect between the interval x and $x+\Delta x$ by

$$\left(\frac{\partial V}{\partial x}\right)_{\rightarrow} \approx \frac{1}{\Delta x} [V_{x+\Delta x,y} - V_{x,y}] \quad (22)$$

The arrow on the partial derivative notes that the approximation is made in the positive or forward direction. This approximation is called the forward-difference approximation.

A backward-difference approximation may be considered as

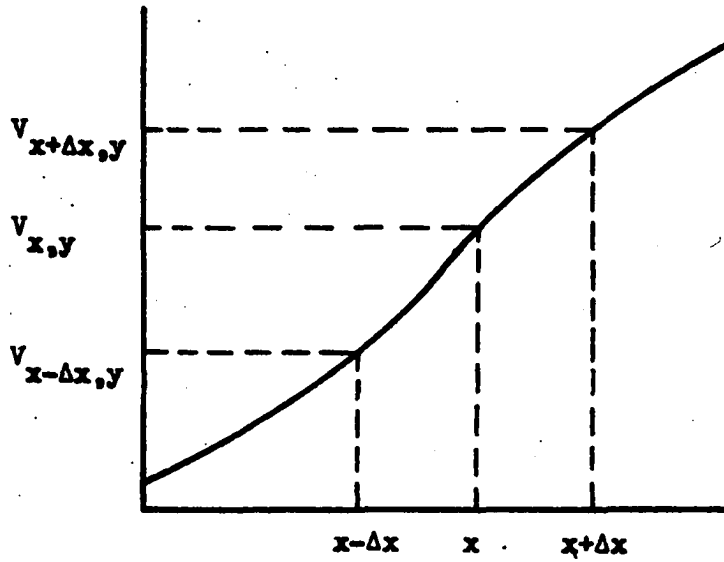


Figure 9. Plot of V versus x -dimension

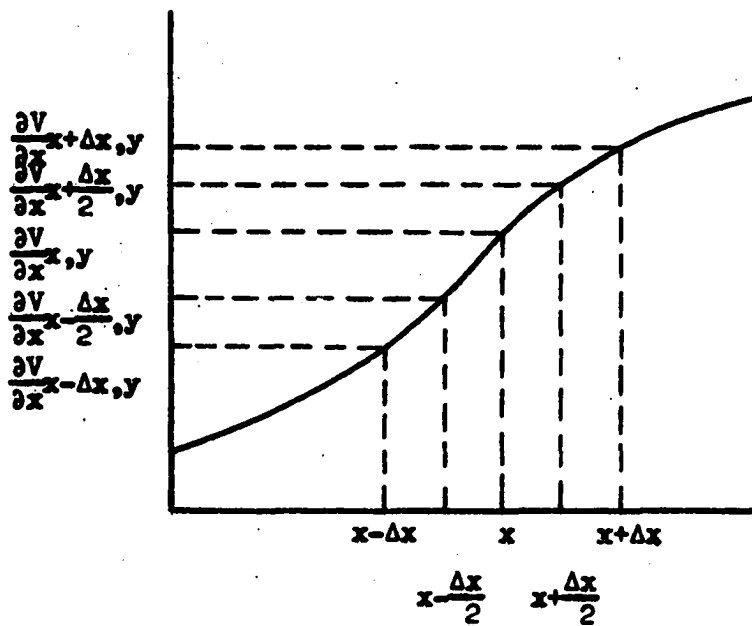


Figure 10. Plot of the partial derivative of voltage with respect to x versus the x -dimension

$$\left(\frac{\partial V}{\partial x}\right)_{\leftarrow} \cong \frac{1}{\Delta x} [V_{x,y} - V_{x-\Delta x,y}] \quad (23)$$

The average-difference approximation is formed by averaging equations 22 and 23.

$$\frac{\partial V}{\partial x} \cong \frac{1}{2} \left[\left(\frac{\partial V}{\partial x}\right)_{\rightarrow} + \left(\frac{\partial V}{\partial x}\right)_{\leftarrow} \right] = \frac{1}{2\Delta x} [V_{x+\Delta x,y} - V_{x-\Delta x,y}] \quad (24)$$

Similarly the various partial derivatives of V with respect to the y -dimension may be formed as the following:

$$\left(\frac{\partial V}{\partial y}\right)_{\uparrow} \cong \frac{1}{\Delta y} [V_{x,y+\Delta y} - V_{x,y}] \quad (25)$$

$$\left(\frac{\partial V}{\partial y}\right)_{\downarrow} \cong \frac{1}{\Delta y} [V_{x,y} - V_{x,y-\Delta y}] \quad (26)$$

$$\left(\frac{\partial V}{\partial y}\right) \cong \frac{1}{2} \left[\left(\frac{\partial V}{\partial y}\right)_{\uparrow} + \left(\frac{\partial V}{\partial y}\right)_{\downarrow} \right] = \frac{1}{2\Delta y} [V_{x,y+\Delta y} - V_{x,y-\Delta y}] \quad (27)$$

Equation 25 is the upward-difference approximation; equation 26 is the downward-difference approximation; and equation 27 is the average-difference approximation.

In order to develop an average-difference approximation for the second partial derivative of V with respect to x in terms of the same interval Δx , consider Figure 10. By considering the average-difference of the derivative of the slope to be only over an interval of Δx , one may define the second partial of V with respect to x as

$$\frac{\partial^2 V}{\partial x^2} \cong \frac{1}{\Delta x} \left[\frac{\partial V}{\partial x} \Big|_{x + \frac{\Delta x}{2}} - \frac{\partial V}{\partial x} \Big|_{x - \frac{\Delta x}{2}} \right] \quad (28)$$

The average-difference approximations of the first partials of V with respect to x at $x + \frac{\Delta x}{2}$ and $x - \frac{\Delta x}{2}$ are the following:

$$\left(\frac{\partial V}{\partial x}\right)_{x + \frac{\Delta x}{2}} \cong \frac{1}{\Delta x} [V_{x+\Delta x,y} - V_{x,y}] \quad (29)$$

and

$$\left(\frac{\partial V}{\partial x}\right)_{x-\frac{\Delta x}{2},y} \cong \frac{1}{\Delta x} [V_{x,y} - V_{x-\Delta x,y}] \quad (30)$$

Substituting equations 29 and 30 into 28, one arrives at the central-difference approximation to the second partial of V with respect to the x -dimension.

$$\frac{\partial^2 V}{\partial x^2} \cong \frac{1}{(\Delta x)^2} [V_{x+\Delta x,y} - 2V_{x,y} + V_{x-\Delta x,y}] \quad (31)$$

Note now that in order to evaluate the first and second partials of V with respect to x , only information about $V_{x,y}$ at the point x,y and V at the chosen increment Δx to the left of and to the right of $V_{x,y}$ need be supplied.

A similar derivation for the second partial of V with respect to the y -direction results in

$$\frac{\partial^2 V}{\partial y^2} \cong \frac{1}{(\Delta y)^2} [V_{x,y+\Delta y} - 2V_{x,y} + V_{x,y-\Delta y}] \quad (32)$$

Laplace's equation for the voltage distribution within the three-dimensional conducting region may be stated as

$$\nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} + \frac{\partial^2 V}{\partial z^2} = 0 \quad (33)$$

Again it is pointed out that the geometries to be investigated will be uniform in the z -direction; hence $\frac{\partial V}{\partial z} = 0$ as well as $\frac{\partial^2 V}{\partial z^2} = 0$.

When the central-difference approximations are applied, Laplace's equation becomes

$$\begin{aligned} \nabla^2 V \cong & \frac{1}{(\Delta x)^2} [V_{x+\Delta x, y} - 2V_{x, y} + V_{x-\Delta x, y}] \\ & + \frac{1}{(\Delta y)^2} [V_{x, y+\Delta y} - 2V_{x, y} + V_{x, y-\Delta y}] = 0 \quad . \end{aligned} \quad (34)$$

Generally in the geometries to be investigated, Δx will not equal Δy ; consequently, a better expression for the voltage $V_{x, y}$ in terms of its four nearest neighbors may be obtained by multiplying equation 34 by $(\Delta x)^2$ and grouping terms as shown.

$$\begin{aligned} (\Delta x)^2 \nabla^2 V = & V_{x+\Delta x, y} + V_{x-\Delta x, y} \\ & + \left(\frac{\Delta x}{\Delta y}\right)^2 [V_{x, y+\Delta y} + V_{x, y-\Delta y}] \\ & - 2\left[1 + \left(\frac{\Delta x}{\Delta y}\right)^2\right] V_{x, y} = 0 \end{aligned} \quad (35)$$

EXPERIMENTAL INVESTIGATION

Solution to Rectangular Bar with Rectangular Cross-section

The first trial described is the rectangular bar with a rectangular cross-section which has a length to height ratio of four to one. What the actual height would be, would be dictated by what pinch-off voltage is desired. Figure 5 or equation 13 determines the design height.

The four to one ratio is not unique---only typical. Ratios from three to one to ten to one cover typical values. A four to one ratio lends itself to a reasonable example.

In all the examples cited, the drain current is assumed to be the same as the source current. This means that the gate junction reverse bias current is zero or at least negligible with respect to the drain current. For typical diodes it is easy to construct p-n junctions with reverse bias currents in the order of 10^{-9} ampere while the forward bias current is in the order of tens or hundreds of milliamperes. Although the pinch-off diode is not the same as a standard semiconductor diode, the currents for reverse bias may be designed to be of the order of magnitude quoted. The drain current may be adjusted in size to be large with respect to the gate current by juggling geometries and materials.

For this trial, Trial I, the resistance will be computed for six values of relative applied voltage. These values will be 0, 0.090, 0.2025, 0.36, 0.64 and 0.81. These values correspond to depletion depth penetrations at the drain end of 0, 0.3, 0.45, 0.6, 0.8 and 0.9 of the way through the bar in the y-direction. Subsequent trials will use the same penetrations since many of the rows of the augmented matrices to be formed

may be used for various geometries.

The grid point system for which the voltages are to be determined is shown in Figure 11. The numbering system for the various voltage points is chosen as shown in order that each new solution for a new voltage level will not require setting up an entirely new augmented matrix. The same rows of the previous matrix will be the same for the new matrix except for the addition or deletion of appropriate zero columns.

Although the penetration varies with the square root of the voltage existing at the location in the x-direction, the voltage in the x-direction is chosen to vary linearly with x. This choice simplifies setting up the finite-difference equations for the lower boundary of the conducting region of the diode for a particular voltage solution.

After a solution has been effected for the potential of all points, the lower boundary predicted by equation 13 is drawn. If it differs appreciably in location or slope from the linear assumption, a new solution is effected incorporating new boundary and slope information.

In the rectangle chosen, Δx is 0.50 unit and Δy is 0.10 unit. The two increments are not chosen equal because a rather closely spaced vertical point location scheme is necessary to see changes in the applied relative voltage. If such a small Δx were used, the number of data points would get out of hand. 429 data points would be necessary, lending themselves to an augmented matrix of 184,470 elements. This size is somewhat beyond the capability of the Cyclone computer.

Actually it will be shown that this choice of Δx and Δy lends itself to solutions which are sufficiently precise. The penetration depths at the drain of 0, 0.3, 0.45, 0.6, 0.8 and 0.9 unit lend themselves to useful

1	2	3	4	5	6	7
•8	•9	•10	•11	•12	•13	•14
•15	•16	•17	•18	•19	•20	•42
•21	•22	•23	•24	•25	•41	•49
•26	•27	•28	•29	•40	•48	•53
•30	•31	•32	•39	•47	•52	•57
•33	•34	•38	•46	•51	•56	•58
•35	•37	•45	•50	•55	•62	•63
•36	•44	•54	•60	•61	•66	•67
•43	•59	•64	•65	•72	•74	•76
•68	•69	•70	•71	•73	•75	•77

Figure 11. The grid point number locations

data points for each solution of 77, 63, 58, 53, 49 and 42 points respectively.

When $\Delta x = 0.50$ and $\Delta y = 0.10$ are inserted in equation 35, equation 36 results.

$$V_{x+\Delta x,y} + V_{x-\Delta x,y} + 25 V_{x,y+\Delta y} + 25 V_{x,y-\Delta y} - 52 V_{x,y} = 0 \quad (36)$$

This equation is the governing equation for all potential points interior to the conducting portion of the diode. The voltage to be evaluated is $V_{x,y}$.

In order to handle voltage points located on the upper physical conducting boundary and lower conducting boundary, one must resort to invoking the current-potential function orthogonality condition. This condition is expressed as

$$\bar{\nabla} V_{x,y} \cdot \bar{n}(x,y) = 0 \quad (37)$$

where $\bar{\nabla}$ is the two-dimensional Laplacian and $\bar{n}(x,y)$ is the unit normal of the equation describing the physical boundary, $f(x,y)$. If the unit normal can be evaluated on the boundary, and in the geometries investigated it can, rather than using the unit normal, one may as well use the normal of $f(x,y)$. Inserting the terms for $\bar{\nabla} V_{x,y}$ and $\bar{\nabla} f(x,y)$ results in

$$\frac{\partial f}{\partial x} \frac{\partial V}{\partial x} + \frac{\partial f}{\partial y} \frac{\partial V}{\partial y} = 0 \quad (38)$$

When one considers the lower boundary to have a linear penetration in the y -direction with respect to the x -direction, $f(x,y)$ may be expressed as

$$f(x,y) = mx-y \quad (39)$$

where m is the slope of the boundary. Equation 38 becomes

$$m \frac{\partial V}{\partial x} - \frac{\partial V}{\partial y} = 0 \quad . \quad (40)$$

For the penetration of 0.3 of the total height at the drain,

$$m = \frac{0.3}{4} = 0.075 \quad . \quad (41)$$

It is not convenient to attempt to express the partials of V with respect to x and y by means of the average-difference approximation. The reason is that, for the lower boundary, $V_{x+\Delta x, y}$ and $V_{x, y-\Delta y}$ are not physically present; however, the backward-difference and upward-difference equations may be used to circumvent this difficulty. Since the number of potential points is large, the error introduced is not significant.

Under this condition, equation 40 becomes for the lower boundary

$$m \frac{\partial V}{\partial x^{\leftarrow}} - \frac{\partial V}{\partial y^{\uparrow}} =$$

$$m \frac{1}{\Delta x} (V_{x, y} - V_{x-\Delta x, y}) - \frac{1}{\Delta y} (V_{x, y+\Delta y} - V_{x, y}) = 0 \quad . \quad (42)$$

If one substitutes in values for Δx and Δy , equation 42 is

$$(5+m)V_{x, y} - m V_{x-\Delta x, y} - 5 V_{x, y+\Delta y} = 0 \quad . \quad (43)$$

This equation works for all slope conditions, even the zero applied voltage where the lower boundary lies along the x -axis.

The upper boundary is evaluated by an equation similar to equation 43. The upper boundary requires that finite-difference equations to the right and to the downward direction be used.

$$(5+m)V_{x, y} - m V_{x+\Delta x, y} - 5 V_{x, y-\Delta y} = 0 \quad . \quad (44)$$

This equation also is satisfactory for all slope conditions, including that boundary condition occurring when the physical boundary lies parallel to the x-axis.

For each depletion depth penetration, the solution was determined by considering the applied voltage to be one per unit volt. For example, when the drain end penetration is 0.3 the height and the applied voltage $0.09 \frac{V}{V_0}$, the applied voltage is one per unit. This choice simplifies the coefficient column of the augmented matrix. It avoids having to manufacture a completely new column for each applied voltage.

The above condition leads to the boundary condition that provides the forcing functions for many of the equations in the total solution.

$$V_{4,y} = 1 \quad (45)$$

A second boundary condition completes the forcing function requirements. This condition notes that the source end of the diode is grounded.

$$V_{0,y} = 0 \quad (46)$$

To illustrate several of the many equations generated by this technique, five equations are shown.

On the interior at location 9

$$-52 V_9 + V_8 + V_{10} + 25 V_2 + 25 V_{16} = 0 \quad (47)$$

On the source end at location 8

$$-52 V_8 + V_9 + 25 V_1 + 25 V_{15} = 0 \quad (48)$$

On the drain end at location 14

$$-52 V_{14} + V_{13} + 25 V_7 + 25 V_{42} = -1 \quad (49)$$

On the lower surface at location 63

$$-5.075 V_{63} + 0.075 V_{62} + 5 V_{58} = 0 \quad . \quad (50)$$

On the upper surface at location 2

$$- V_2 + V_9 = 0 \quad . \quad (51)$$

After the entire set of equations has been generated, an augmented coefficient matrix is formed. For the example to be followed through, the condition where the drain end depletion depth is 0.3, the matrix is 63 by 64. The matrix contains 4032 elements; however, most are zeros since the maximum number of non-zero entries in any row can be five. This situation eases the tape preparation for the Cyclone computer, but does not speed the solution time perceptibly.

The program used is a SAR program already existing called M14A. Briefly the coefficients are fed in one row at a time. As a row is accepted, it is normalized and operated upon such that the matrix is diagonalized. When the last row has been accepted, the program then begins solving for the unknown potentials, last one first.

It might be pointed out that it is possible to solve for the unknowns by guessing their values and then iterating to the correct set. Programs exist for this type of solution; however, those for the Cyclone computer have a break-even time for about one hundred equations. Below one hundred, triangularization is better; above one hundred, iteration is better. The biggest set of equations used numbered 85.

A 42 equation set takes about five minutes from program input to data tape output. A 77 equation set takes about twelve minutes.

The data point voltage values for the example cited are shown in

Figure 12. For any particular column of data points, the data points do not vary appreciably. As the penetration becomes deeper, the variation becomes more marked.

The actual lower boundary is determined by means of a normalized version of equation 12. It is shown in Figure 12. This boundary is in quite good agreement with the assumption of a linear depth variation.

As the drain end depletion depth becomes greater, the deviation from a linear relation becomes more. If the deviation were sufficient to warrant, the lower boundary slopes at each boundary point can be adjusted to reflect the first solution at a particular drain end depth. In addition data points can be deleted or added if necessary.

In trial I, the slopes were corrected in the solutions for depths of 0.8 and 0.9. The new voltages shifted only about two percent for this geometry; as a consequence, the minor slope deviation of Figure 12 was not judged significant to warrant correction. For other trials it was.

In order to obtain the voltage profile in the x-direction across the diode, the nine data points of the upper boundary and the nine of the lower boundary were plotted as functions of distance across the diode. From the resulting curve shown in Figure 13, the voltage every 0.05 of V_0 was plotted to form Figure 14. This plot is sufficient to speculate on the curvilinear squares and, in turn, the resistance.

For each interval between equipotential lines, the average spacing was measured along with the average height of the area involved. The division of the latter number by the former resulted in a value s for that segment. All of the values s for all 20 intervals were then averaged. In this example \bar{s} equals 4.09.

0.00	.100	.205	.320	.441	.570	.705	.849	1.00
	.100	.205	.320	.441	.570	.705	.849	
	.100	.205	.319	.441	.570	.705	.849	
	.100	.204	.319	.441	.569	.705	.848	1.00
	.099	.203	.318	.440	.568	.704	.847	
0.00	.098	.201	.317	.439	.567	.702	.846	
	.097	.199	.316	.437	.566	.701	.844	1.00
	.096	.196	.314	.436	.564	.696	.842	
	.095	.193	.312	.434	.562			
0.00	.094	.188						

Figure 12. The data point values for Trial I with depletion layer depth at drain of 0.30

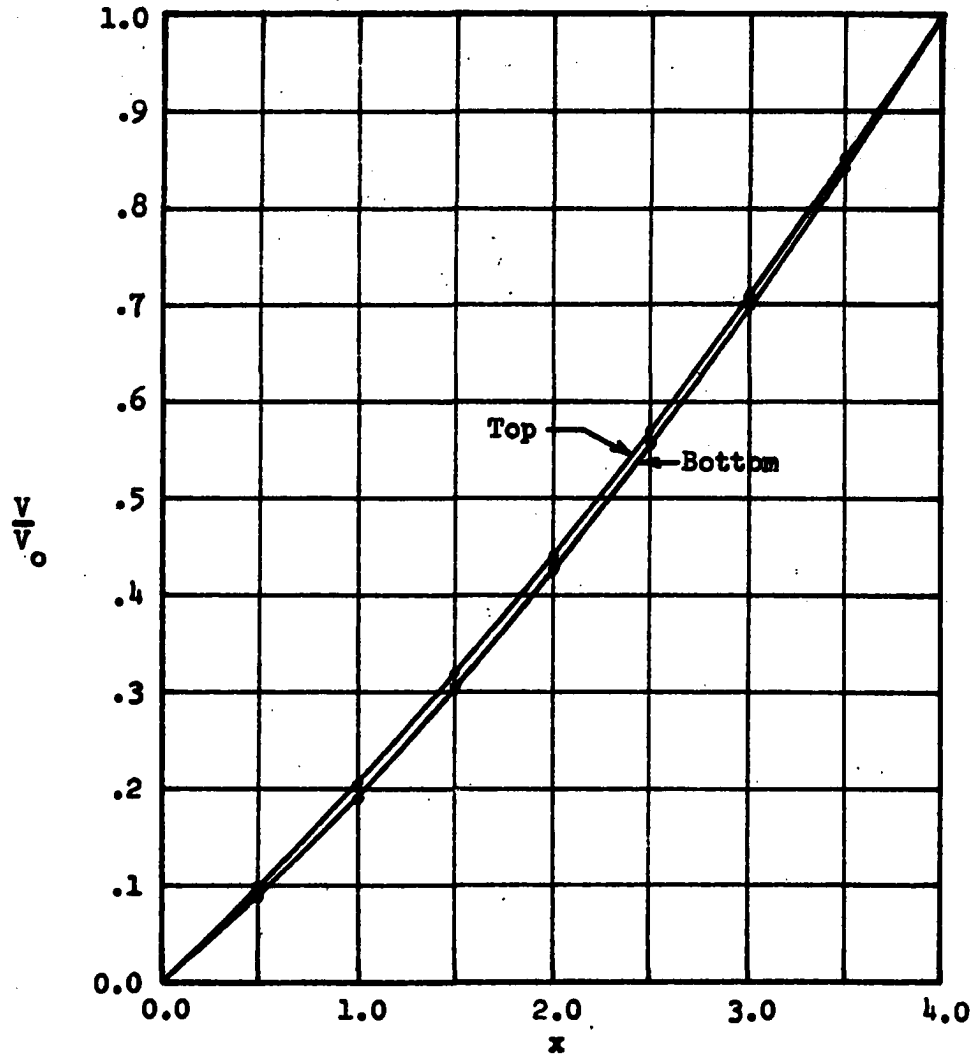


Figure 13. Plot of relative potential versus x for $\frac{V}{V_0}$ equal to 0.09.

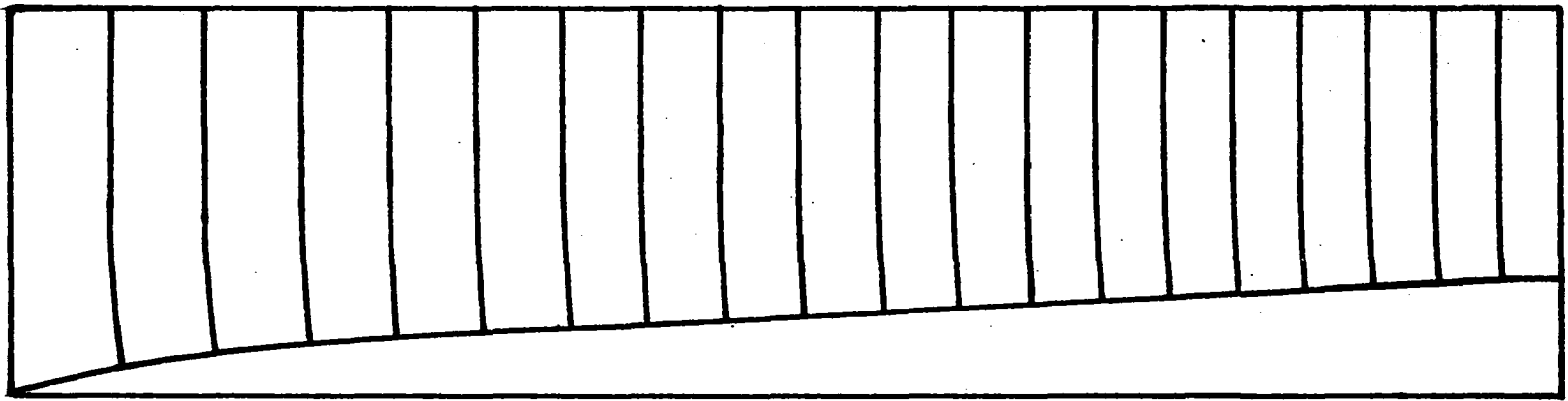


Figure 14. Equipotential lines for intervals of $0.05 V_0$ for drain end penetration of 0.30 of Trial I

The resistance of this configuration is evaluated by equation 21.

\bar{s} is used rather than s . n is 20 and \bar{s} is 4.09

$$\begin{aligned} R &= \frac{20}{4.09} \frac{\rho}{z_0} \\ &= 4.88 \frac{\rho}{z_0} . \end{aligned} \quad (52)$$

The voltage applied is $0.09 V_0$; therefore, the current I resulting is

$$\begin{aligned} I &= \frac{V}{R} = \frac{0.09 V_0}{4.88 \frac{\rho}{z_0}} \\ &= 0.01845 V_0 \frac{z_0}{\rho} . \end{aligned} \quad (53)$$

Similar solutions, graphical construction and calculations result in the plot of resistance versus normalized voltage for Trial I as shown in Figure 15. This curve is useful in determining current-voltage values in regions for which data points do not exist, especially in the region between 0.00 and $0.09 V_0$.

Figure 16 shows the current-voltage relationship for Trial I on a logarithm plot. The geometry of a rectangular bar with a rectangular cross-section lends itself to a current-voltage relationship of the form

$$I = K V^{\frac{1}{h}} \quad (54)$$

where K is a normalization constant and h is 1.22 for the range of voltage from 0.05 to $0.40 V_0$. The dashed line on Figure 16 shows the slope of a characteristic which obeys a $V^{\frac{1}{2}}$ relation. This slope is the desired one and the one to which trials will be pointed.

If one solves the rectangular bar with rectangular cross-section assuming the length is much greater than the height, equation 55 results.

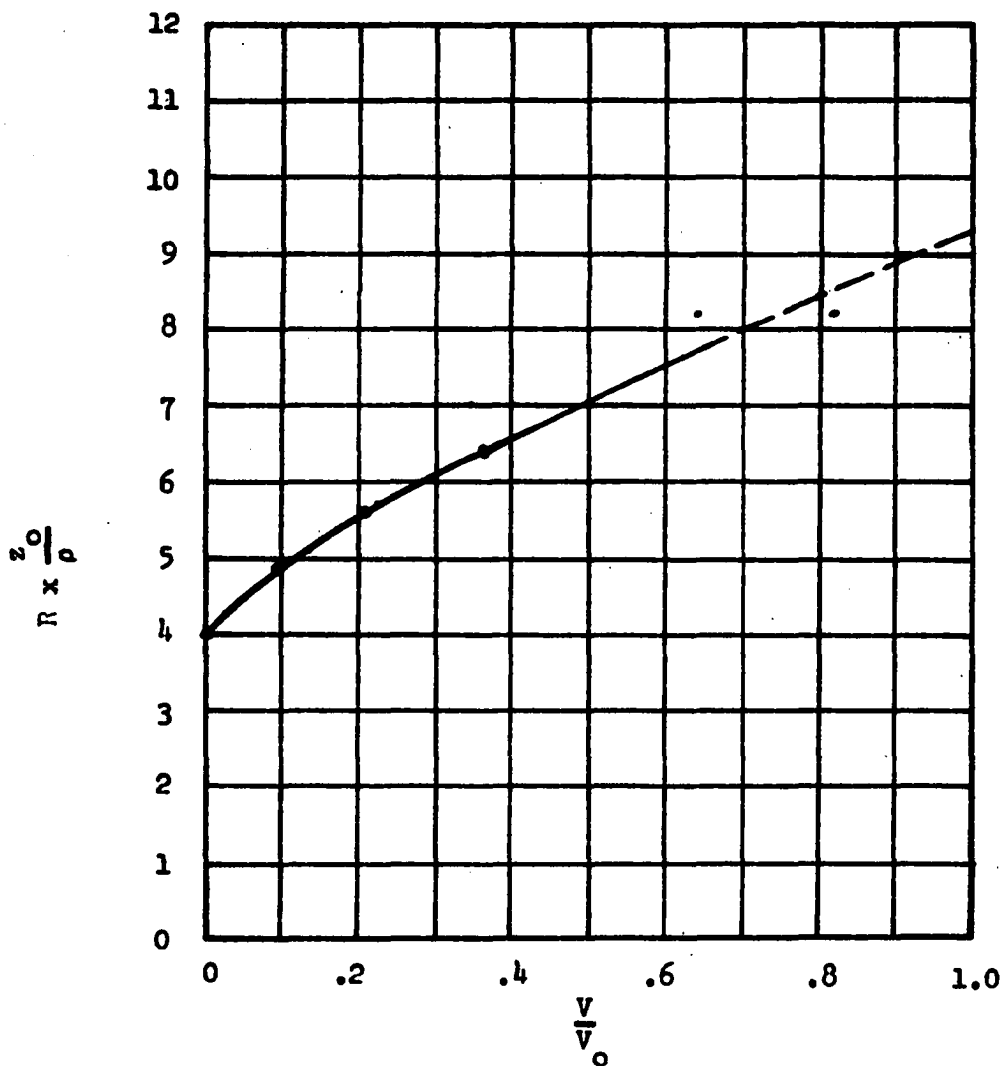


Figure 15. Resistance versus $\frac{V}{V_0}$ for Trial I

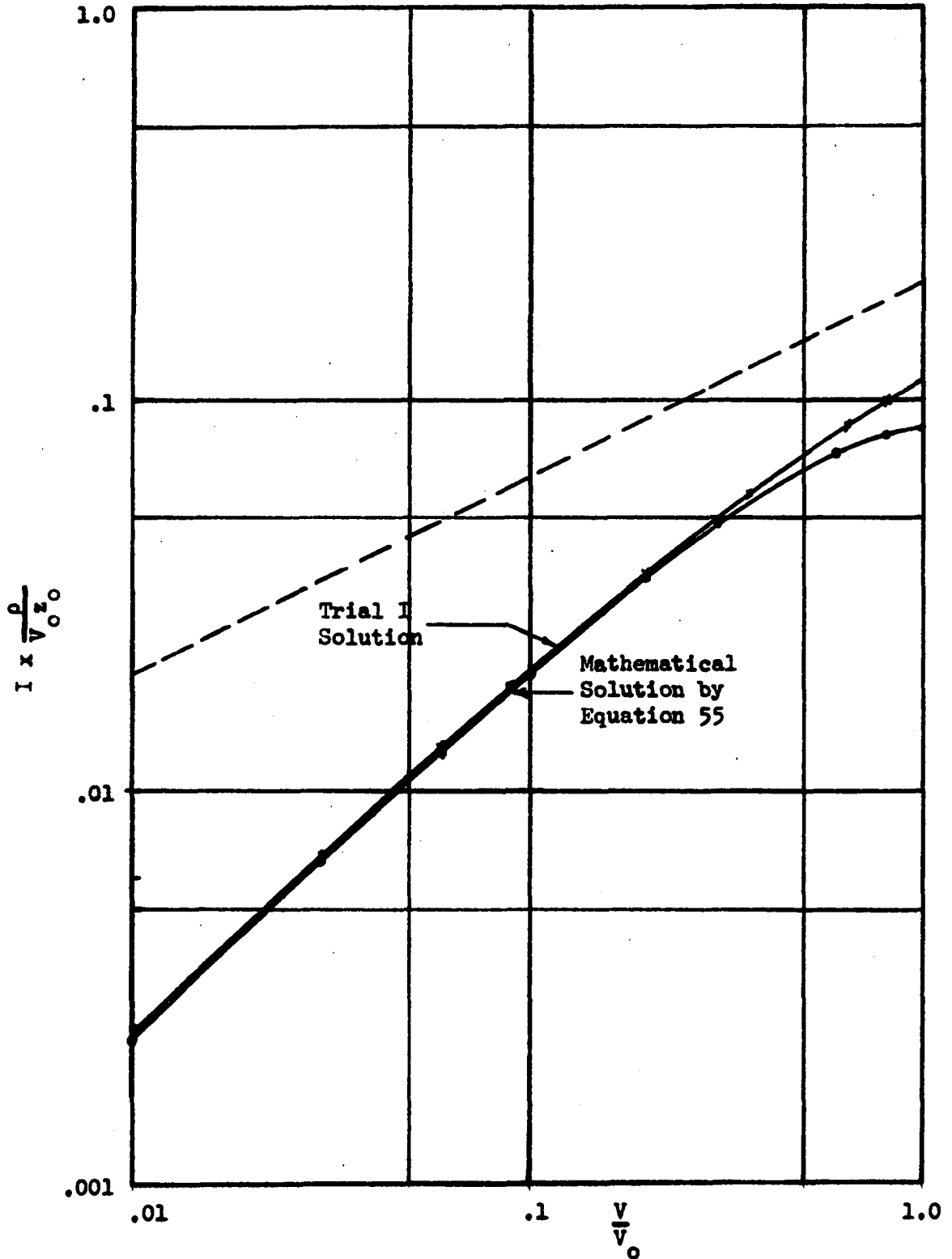


Figure 16. Comparison of mathematical solution and curvilinear squares solution for rectangular configuration

This relation will be derived in Appendix B.

$$I = \frac{z_0 a}{\rho L} V_0 \left\{ \frac{V}{V_0} \left[1 - \frac{2}{3} \left(\frac{V}{V_0} \right)^{\frac{1}{2}} \right] \right\} \quad (55)$$

If the ratio of a to L is made one to four as in the geometries considered, equation 55 plots as shown in Figure 16. The solution by curvilinear squares and the mathematical solution track each other very well up to about $0.40 V_0$. This voltage corresponds to a drain end penetration of 0.633 and is about as far as one would be inclined to use this device. Over this interval these two methods agree within at least four percent, a very satisfactory correlation.

Below the 0.633 value, the mathematical solution is probably quite accurate since the constant voltage profiles are virtually normal to the x -axis. This condition is necessary for a proper solution.

Above the 0.633 value, the constant voltage lines begin to skew appreciably. The accuracy of the solution deteriorates.

Which curve is the correct one is questionable above $0.40 V_0$. The correct solution probably lies between the two, more likely nearer the curvilinear square solution. Since the diodes proposed will not be driven above $0.36 V_0$, this problem was not rationalized.

Solutions to Other Configurations

From the geometrical configuration of Trial I, the desired current-voltage function was developed by gradually changing the physical shape of the diode in the x - y plane. As before the cross-section in the y - z plane is rectangular.

The geometry of the second trial, along with those of subsequent

trials, is shown in Figure 17. Trial II is similar to Trial I except that the upper left-hand corner is shaved off. The sloping physical boundary is linear and passes through the points of $(0,0.6)$ and $(2.75,1)$ in the x - y plane. The source end height of 0.6 is chosen just to show a deviation from Trial I.

The coordinate $(2.75,1)$ is chosen for convenience. This fact points out the notion that the solution is not unique, just one of many. Since the potential distribution is effected by discrete data points, moving the sloping boundary intersection over to $(4,1)$ leads to some mathematical difficulties. They are not impossible but inconvenient. For one thing it is highly likely that the depletion layer depth will punch through the upper boundary at some location other than the drain before V_0 is reached. This situation is not too desirable.

The resulting current-voltage curve for Trial II is shown in Figure 18. Its value for h of equation 54 is 1.24. Although the change in h from Trial I is not great, it does show the direction to proceed.

Trial III is shown in Figure 17. This geometry is of little value other than to show conclusively that changes in the direction of Trial II are necessary. The current-voltage characteristic of Trial III, as shown in Figure 18, has a value of h of 1.17.

Trial IV has a geometry which results in a source end height of 0.3. The current-voltage characteristic shows a marked shift in the direction of the h value of 2.00 desired. The value for h for Trial IV is 1.60.

Trial V has a geometry which results in a source end height of 0.2. The solution is not a complete one since the depletion layer depth penetrates the upper boundary at the coordinate $(0.7,0.4)$ when a voltage of

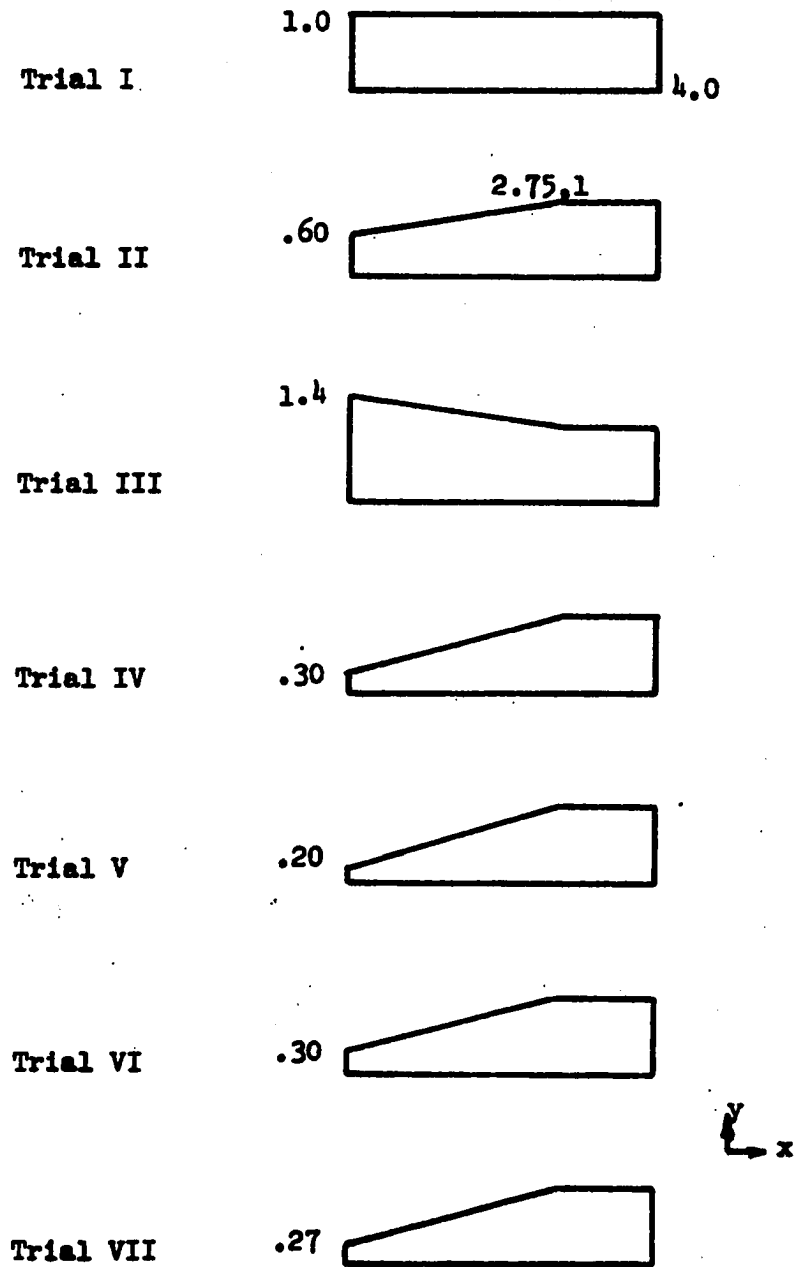


Figure 17. Profile of x-y plane of pinch-off diode for various trials

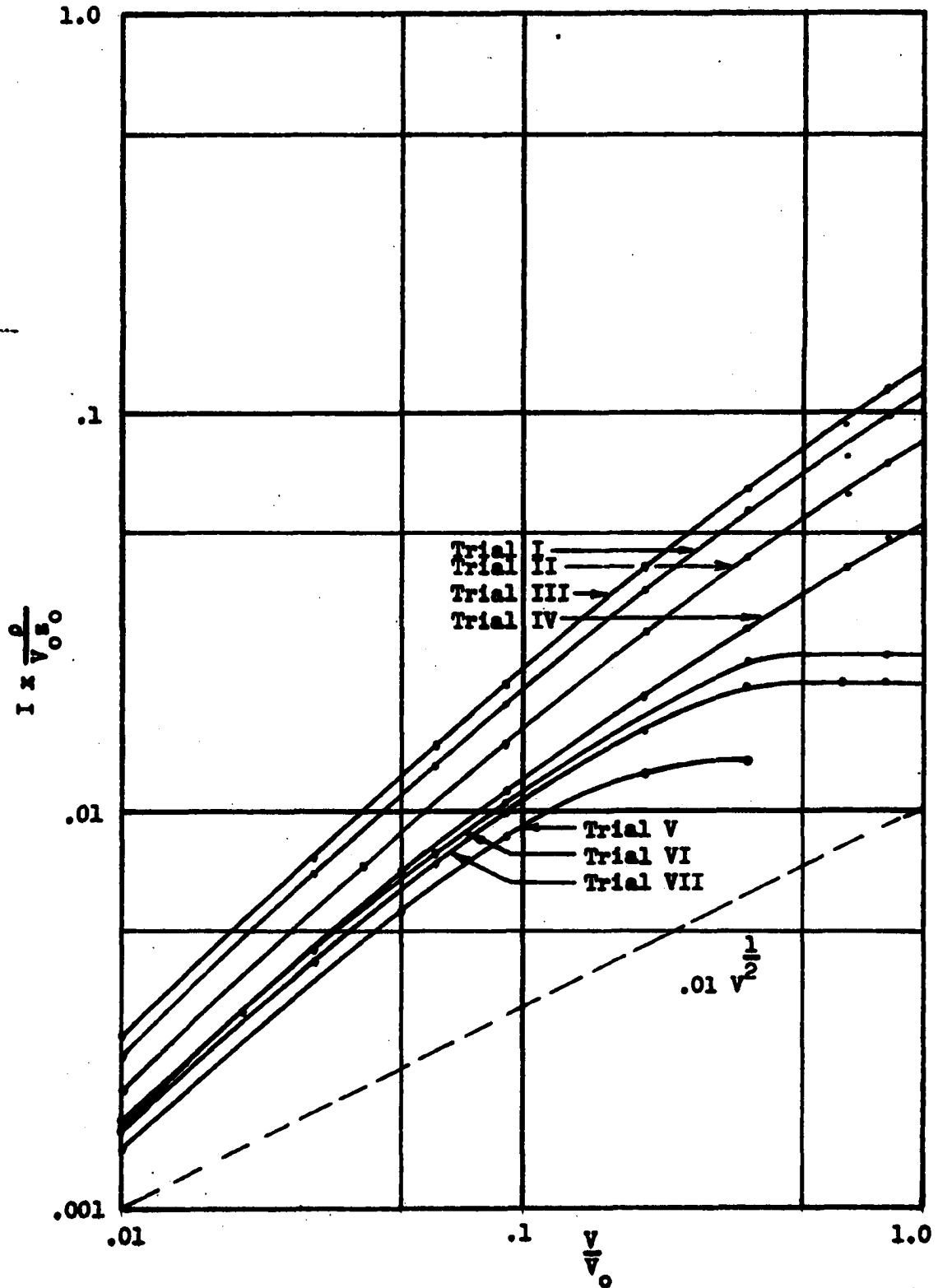


Figure 18. Current-voltage curves for various trials

about $0.42 V_0$ is applied. Note, however, that the value of h for applied voltages between $0.09 V_0$ and $0.36 V_0$ is greater than 2.00.

Trial IV is a solution which assumes that the lower depletion layer boundary is a linear function of the x -displacement for a given drain voltage. This assumption is a good one for Trial I; however, as the upper left corner is removed, the assumption becomes less acceptable.

Trial VI is a solution involving the same geometry as Trial IV. The lower conducting boundary created by the depletion layer depth is adjusted for both slope and location. Some data points are removed to reflect a deeper depletion layer penetration than the linear variation predicts. The resulting current-voltage characteristic is in Figure 18. The value for h of equation 54 is 1.60 for drain voltages between $0.09 V_0$ and $0.36 V_0$.

Trial VI is not a complete solution as not all data points were generated. The reason for this is that the general effect of the slope and data point correction was the prime interest. That h is 1.60 is heartening.

Trial VII is a minor change from Trial VI. The only change is that the source end height is now 0.27. The lower boundary has been corrected for slope and data point content. The current-voltage characteristic of Figure 18 has a value for h of 1.86 for drain voltages between $0.09 V_0$ and $0.36 V_0$.

If one takes all of the resistances generated for the various trials and plots them as a function of the source height with the drain voltage as a free parameter, he can speculate quite adequately about the resistances occurring for source heights of 0.26 and 0.25 when the drain voltage

is varied. These resistances for various drain voltages can be used to generate current-voltage characteristics. An example is shown in Figure 19.

The equations of curves fit by the least squares method for source heights of 0.27, 0.26 and 0.25 are respectively the following:

$$I = 0.0366 V^{\frac{1}{1.86}} \quad (55)$$

$$I = 0.0336 V^{\frac{1}{1.96}} \quad (56)$$

and
$$I = 0.0304 V^{\frac{1}{2.11}} \quad (57)$$

The curves are valid in the range $0.09 V_0$ to $0.36 V_0$. The desired value of h is bracketed between a source height of 0.26 and 0.25. The precision of the overall solution does not warrant effecting a solution for a source height for h of exactly 2.00.

The dashed curve of Figure 19 is a plot of the equation

$$I = 0.033 V^{\frac{1}{2}} \quad (58)$$

The values of the current-voltage curve for the source height of 0.26 deviate less than 3.25 percent from the values predicted by equation 58. It is concluded that a geometry like that of Trial VII except for a source height of 0.26 would be a satisfactory square law detector over the range 0.09 to $0.36 V_0$ when the device is driven by a current.

Improvement of Characteristics by Gate Current and Shunt Path

With the geometries and materials chosen, it is not possible to make a pinch-off diode characteristic which follows a $V^{\frac{1}{2}}$ law to voltages near

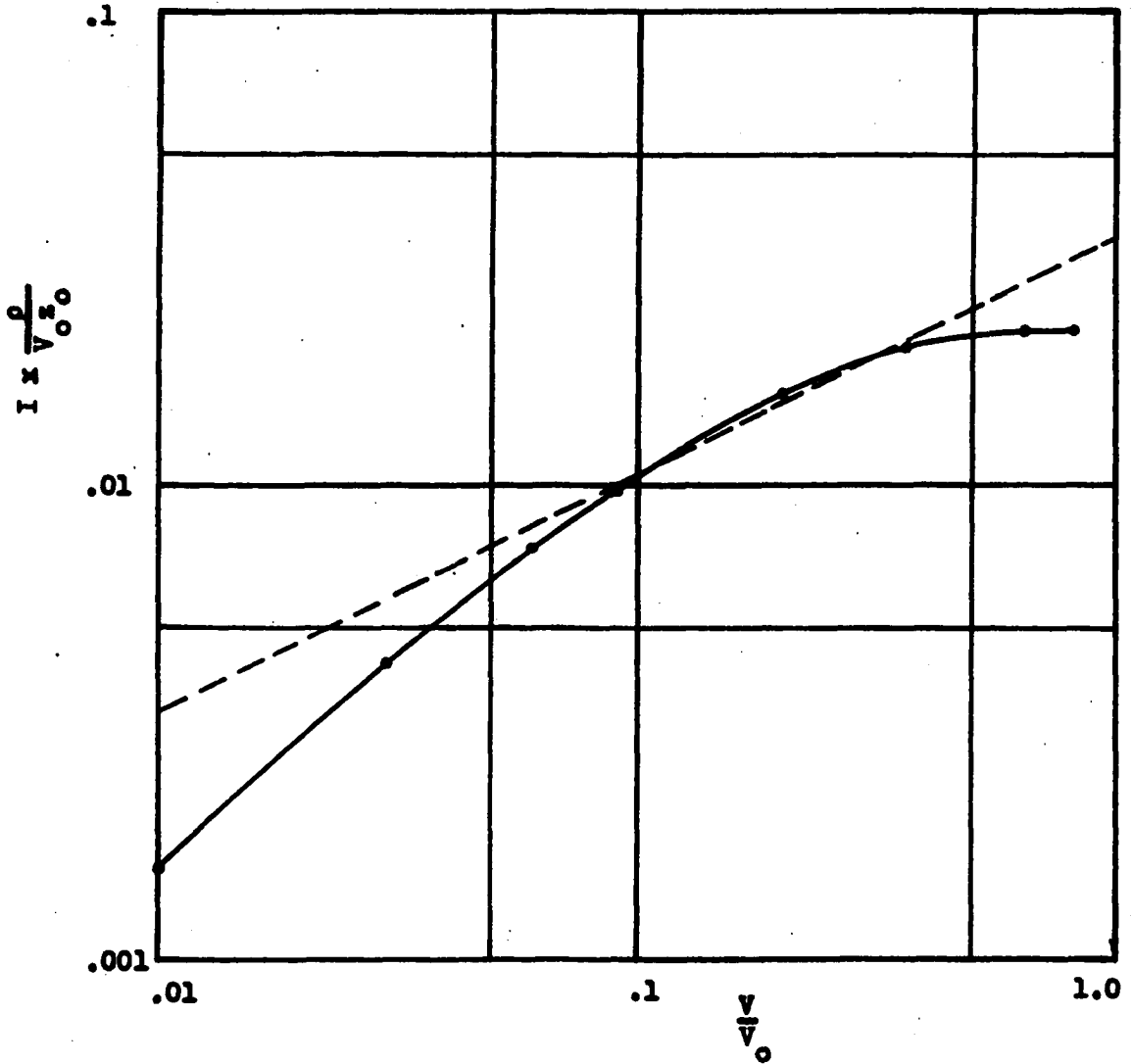


Figure 19. Current-voltage curve for pinch-off diode with source end dimension of 0.26

zero. To have one that would require a device which exhibits zero resistance at zero applied voltage. None of the ones described does; as a consequence, one must resort to an incremental device or else settle for an appreciable error in current value near zero applied voltage.

The diodes discussed are designed with the restriction that the gate current is zero or negligible with respect to the drain current. Such diodes are readily designed. The question that now arises is the following: can the current-voltage characteristic of a diode possessing no gate current be improved by designing a new diode, geometrically the same, but with gate current?

The current-voltage characteristic of Trial VII is plotted in Figure 20. Also is plotted the equation $I = 0.025 V^{\frac{1}{2}}$. When the difference of the two curves is plotted the dashed curve results. Except for values very near zero drain voltage, this dotted curve can be reasonably approximated by a constant current of $0.0013 \frac{V_0 z_0}{\rho}$ amp and the current resulting from a resistance of $250 \frac{\rho}{z_0}$ ohms shunting the diode.

When the constant current and current from the shunt resistance are summed with the current-voltage characteristic of Trial VII, the resultant current-voltage characteristic is generated. This resultant curve is of value since it will follow a $V^{\frac{1}{2}}$ curve within five percent of the full-scale current value if full-scale is considered at $0.36 V_0$.

In many cases this tracking would be wholly satisfactory. A great advantage is that a device now exists which may be driven successfully from zero voltage if desired. A somewhat greater voltage range is also available.

The tracking is within five percent. A slight increase in the

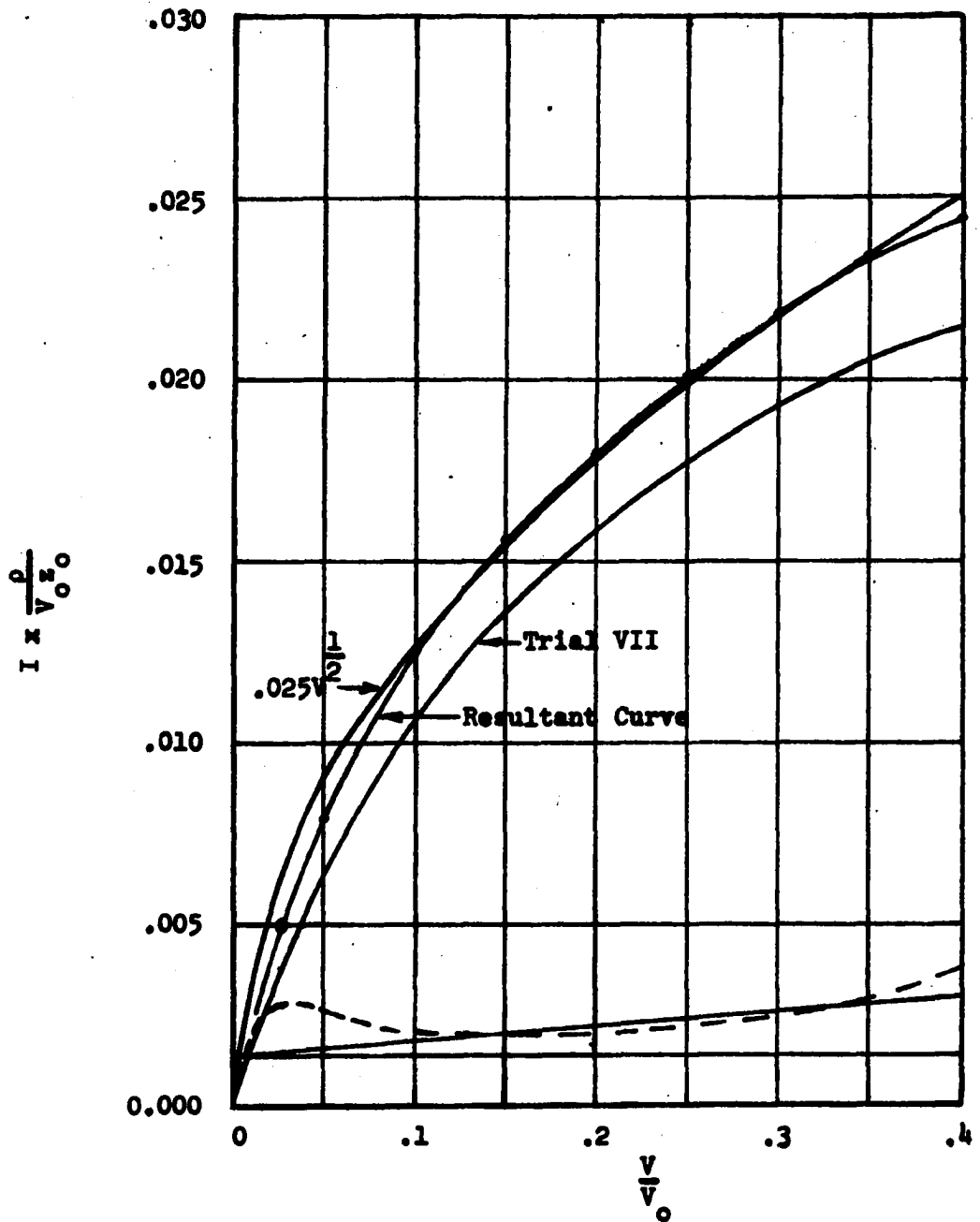


Figure 20. Formation of $I = K V^{\frac{1}{2}}$ characteristic by means of gate diode current and shunt path

constant current and a corresponding increase in shunt resistance will improve the tracking.

The constant current may be derived from designing the gate current to be appreciable with respect to the drain current. To effect this design, it may be necessary to actually lower the drain current by material and geometrical considerations to values where it is only about twenty times the gate current. This consideration should not affect the current-voltage characteristic of Trial VII appreciably.

A reverse biased p-n junction such as the gate junction exhibits a reverse bias characteristic of

$$I_d = I_s \left(1 - e^{-\frac{qV}{KT}} \right) . \quad (59)$$

I_d is the reverse bias current, I_s the reverse bias saturation current, K Boltzmann's constant and T the absolute temperature. Generally the diode equation is expressed as the negative of equation 59. Equation 59 is given in terms of the voltage and current polarities of the pinch-off diode.

Whenever the applied voltage V to the reverse biased diode becomes more than a few tenths of a voltage, the exponential term of equation 59 becomes small compared to one under normal temperature conditions. Generally V_o of the pinch-off diode will be between 10 and 100 volts; consequently I_d may be treated as a constant I_s . By allowing gate current, the constant current of the graphical construction of Figure 20 may be realized.

Nanavati (13) derives the equation for I_s .

$$I_s = q A \left(\frac{D_p p_n}{L_p} + \frac{D_n n_p}{L_n} \right) . \quad (60)$$

A is the p-n junction area, D_p the diffusion constant for holes, D_n the diffusion constant for electrons, L_p the diffusion length for holes, L_n the diffusion length for electrons, p_n the concentration of holes in the n-type material, and n_p the concentration of electrons in p-type material. The diffusion constants and diffusion lengths are peculiar to a particular semiconductor material and are not the same for holes and electrons.

If one wished to incorporate gate current compensation into a pinch-off diode design, he would be inclined to shift from silicon to germanium since the latter has a higher I_s , all other conditions being equal. In fact I_s for a germanium p-n junction is about 1000 times that for a similar p-n junction of silicon. Typical p-n junctions of germanium have I_s values around 100 microampères.

The use of gate current compensation may lead to some difficulties. The pinch-off diode with no or negligible gate current is a majority carrier device; consequently, it is temperature insensitive over reasonable temperature ranges.

Both terms in the expression for I_s contain factors representing minority carrier concentrations--- n_p and p_n . These quantities are quite temperature sensitive; therefore, the amount of gate current compensation varies with temperature. The current-voltage characteristic varies with temperature.

Whether this problem is serious depends on the design requirements. If it is, it may be necessary to insure constant temperature operation,

to temperature compensate, or to abandon gate current compensation.

In order to get I_s up to levels approaching five percent of the desired source current levels, one may attempt to increase the gate junction area A of equation 59. Increasing A increases both the drain current and the gate junction reverse bias capacitance. The increase in drain current defeats the attempt to relatively increase the gate current. Any relative increase will have to come from the material considerations of equation 59.

Increasing the gate junction capacitance deteriorates the frequency characteristics of the pinch-off diode. Perhaps a compromise will have to be effected in this respect. The next section will shed some light on the frequency capability expectations of the pinch-off diode.

Predicted Frequency Characteristics

A reverse biased p-n diode exhibits a junction capacitance created by movement of the depletion layer when the voltage across the junction is varied. Capacitance is defined as

$$C = \frac{dQ}{dV} \quad (61)$$

which may be rewritten as

$$C = \frac{dQ}{db} \cdot \frac{db}{dV_b} \quad (62)$$

Q is the charge that exists in the depletion region.

From Figure 4, it may be seen that

$$\frac{dQ}{db} = A q N_d \quad (63)$$

where A is the area of the p-n junction. The value of b in terms V_b may

be obtained by regrouping equation 11 after the employment of equation 9.

It is expressed as

$$b = \left[\frac{2\epsilon}{q N_d} \left(1 + \frac{N_d}{N_a} \right) \right]^{\frac{1}{2}} V_b^{\frac{1}{2}} . \quad (64)$$

From this equation it follows that

$$\frac{db}{dV_b} = \left[\frac{\epsilon}{2q N_d} \left(1 + \frac{N_d}{N_a} \right) \right]^{\frac{1}{2}} V_b^{-\frac{1}{2}} \quad (65)$$

and

$$C = A \left[\frac{\epsilon q N_d}{2 \left(1 + \frac{N_d}{N_a} \right)} \right]^{\frac{1}{2}} V_b^{-\frac{1}{2}} . \quad (66)$$

If $N_a \gg N_d$, as is the case described, the factor containing N_a and N_d in the denominator becomes unity.

The capacitance per cross-sectional area of the junction may be obtained from Figure 5. A similar capacitance expression for the case when $N_d \gg N_a$ may be developed by employing equation 66. Its variation is the same on Figure 5 as that of equation 66 with the $N_a \gg N_d$ inequality invoked.

In order to obtain a relative feel for the upper frequency limit for a device of this type, it is well to look at the sizes and quantities involved. Suppose it is desired to make a pinch-off diode like that of Trial VII but with a source height of 0.26. The voltage between 0.10 V_0 and 0.36 V_0 is desired to be 10 volts. This situation requires that V_0 be about 40 volts. The n-type channel material is chosen to have a resistivity of one ohm-meter.

Figure 5 shows that the drain and height must be 47×10^{-6} meter. The base would be 188×10^{-6} meter.

For this device, Figure 19 shows that for $0.10 V_0$, the $I \times \frac{\rho}{V_0 z_0}$ equals about 0.010. A choice for z_0 of 100×10^{-6} meter leads to a current of 40 microamperes. This value is typical of the current levels involved.

The cross-sectional area of the p-n junction is approximately 1.88×10^{-8} meter. If one assumes that $0.2 V_0$ is applied and that the average voltage on the junction is about $0.1 V_0$, Figure 5 gives a capacitance per area value of 10.5×10^{-6} farad per meter². The junction capacitance is 0.19×10^{-12} farad under these assumptions.

For the same $0.2 V_0$, Figure 19 gives a current value which results in a series resistance value of $12.9 \frac{\rho}{z_0}$ or 1.29×10^5 ohms.

A normal reverse biased p-n junction usually is represented by a shunt capacitance, a very large shunt resistance and a constant current generator. A normal diode in this instance is one that has the current flow normal to the junction area. Under this circumstance the depletion layer depth is uniform for a given reverse bias. All of the circuit representations may be described adequately.

In the pinch-off diode the main current flow is more or less parallel to the p-n junction; consequently, the voltage across the face of the junction, the depletion layer depth, the capacitance per area, and the resistance per unit length all vary from drain to source. No single constant can be used to describe any particular quantity.

For the example cited, the current generator has been suppressed by design. The shunt resistance may be neglected with reasonable assurance that no significant error will be introduced. The equivalent circuit of

the device is a distributed series resistance with a distributed capacitance to ground. Both distributed quantities vary with the x-distance.

This problem is difficult to solve accurately. Extreme accuracy is not warranted since the capacitances involved are picofarads. Unaccountable strays will severely impair any accurate solution.

One method to solve for a cut-off frequency is to divide the diode into equal parts with respect to distance along the junction in the general x-direction. To each region ascribe a tee-network composed of a representative capacitance bridged by two representative resistances. Figure 21 shows the resultant network. As n becomes large, the cut-off frequency should approach the actual value.

A very pessimistic value, predicted by n equal to three, is a cut-off frequency of about 8.5×10^6 cycles per second. If n is increased to seven the cut-off frequency predicted increases to 12.35×10^6 cycles per second. Neither number is the correct value; however, they point out the order of magnitude involved for a device of this nature. It is likely that the devices could be designed for use to about 25×10^6 cycles per second. The numbers involved here are not significantly different from cut-off frequencies associated with early field-effect transistors (15).

It should be noted that, once a height to length ratio has been chosen, no design other than material can help increase the usable frequency limit. As the area of the diode junction is reduced to lower the junction capacitance, the series resistance increases. Both depend upon z_0 .

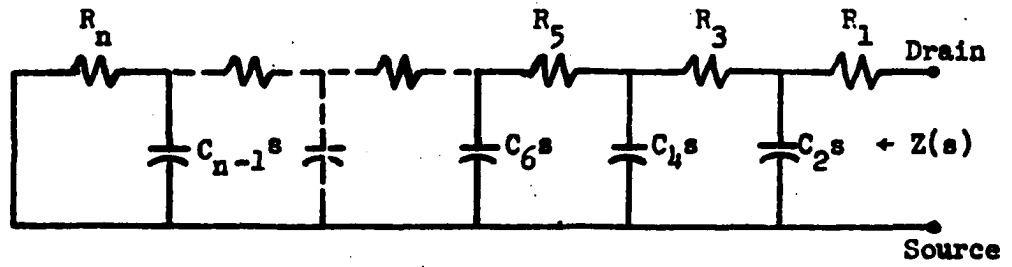


Figure 21. Lumped parameter equivalent circuit of pinch-off diode

Proposed Construction Method

The pinch-off diode like that described in Trial VII except for a source height of 0.26 could be fabricated relatively easily provided that sufficient precision fabricating facilities are available. Numerous techniques, each having its advantages, are available to the semiconductor fabricator. A three volume set authored by members of the Bell Telephone Laboratories describing many techniques developed for germanium and silicon offers a wealth of information (2,3,7).

Once a paper design has been completed, the various material considerations, such as kind and conducting channel resistivity, are fixed. Actual design sizes are also fixed.

The first step in the fabrication process would be to carefully cut a slice of semiconductor to the approximate thickness; it would be cut oversize since cutting is a grossly macroscopic process so far as semiconductor theory is concerned. The slice would be lapped to flatten the faces and then polished to as fine a finish as possible.

Ideally, the surfaces of the slice would be made up of one layer of ions of the semiconductor lattice. In practice this type of surface is not obtainable; however, the smoothest that is obtainable is attempted. Mechanical polishing is still rather crude and chemical polishing is used.

For semiconductors, chemical polishes are very caustic etches, usually containing hydrofluoric, nitric, and sulphuric acid along with iodine in some (10). From the rather matte surface obtained from mechanical polishing, a shiny surface, the best obtainable, can be obtained from chemical

polishing. By experimental processes, one may determine what slice thickness must be cut in order to arrive at the proper drain height after mechanical and chemical polishing have been accomplished.

The next step would be to form the p-n junction. Since the slice may be in the order of an inch in diameter, it may be advisable to make a large area p-n junction. After it is fabricated the slice will be cut or scored and broken to form many small area p-n junction diodes.

The process involved in forming p-n junctions can be alloying, diffusing or vapor depositing. If small voltage diodes are of interest, resistivities would be low and alloying or diffusion would be practical. As the voltage levels necessary by design criteria become high, resistivities become high and vapor depositing becomes more necessary.

All of the types of junction formation involve rather high temperature heat processes. Generally for a given process, material and size of slice, experimental metallurgical processes will have to be developed.

Once the p-n junction is formed, areas exactly the area of the p-n junction in the x-z plane of Figure 3 are defined. Again, many areas may be readily defined simultaneously. The process involved is a photolithographic one (11).

The p-type surface is coated with some material such as KPR. KPR is a light sensitive emulsion that, after exposure to light and development, is resistive to milder varieties of the chemical etches. The coated slice is masked by a highly reduced photo negative which has the diode area or areas on it. Exposure to ultraviolet light, development and etching result in the definition of area or areas in the x-z plane.

If multiple diodes are made on the slice, they would now be separated.

Depending on the sizes of the area of the diode p-n junctions, slicing, air abrasive cutting or diamond scribing and breaking can be used to separate the individual pinch-off diodes.

Throughout all of the preceding processes and those to follow cleanliness is a paramount requirement. If the p-n junction boundary edges are not kept clean, significant leakage paths develop. These may destroy the design which is being attempted.

The p-n junction is now mounted to a mounting tab to facilitate its handling. It could be glued with epoxy or soldered. Since a good electrical connection is desirable from the outer p-type face of the gate junction to the source, conducting epoxy or a low resistivity solder can be used. Care must be used in conducting epoxy or solder selection. Since the material must link p-type and n-type semiconductor material, it must be carefully chosen to look ohmic to both.

Lead wires are now attached to the source and drain. Although not important to the source, the lead for the drain should be attached as shown in Figure 3. The reason is that the drain voltage must be dropped from the drain contact to the upper surface of the depletion layer of the gate diode. By placing the contact as shown, the distance involved is the maximum available. Maximizing this distance minimizes leakage currents around the drain end. The contact location also allows a maximum penetration of the depletion layer if desired.

The next step is the most critical. It involves removing the semiconductor material which is enclosed in the volume defined by the right triangle in the x-y plane which has coordinates (0,1), (0,0.26) and (2.75,1) and extends back a distance z_0 . Figure 22 illustrates the

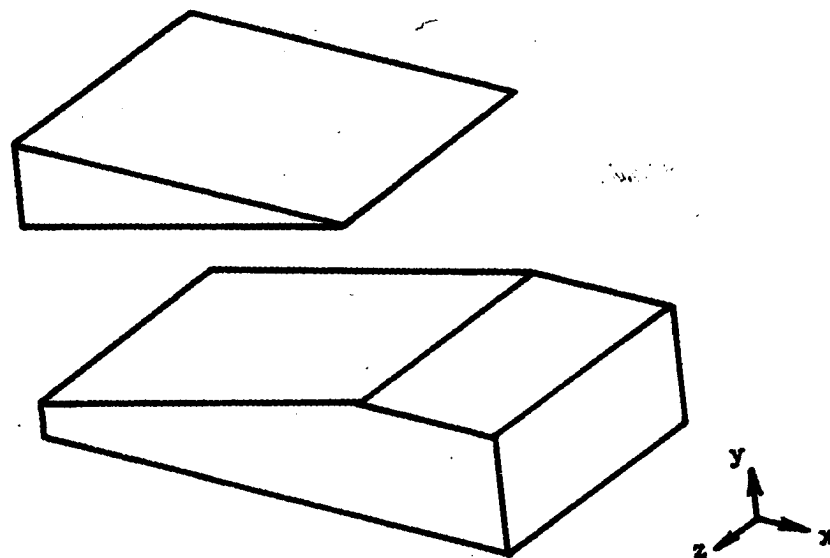


Figure 22. Material to be removed from diode body

material to be removed from the diode body.

Several methods for removal are possible. If the diode is of sufficient size, the material can be mechanically polished off and then re-etched chemically. If each diode is made separately it may be possible to cut the original slice with faces not parallel. The angle between the slice faces would be representative of the volume removed.

The most probable method is to mask the diode and to electro-chemically etch the material away. The advantage of this method is that very small dimensional tolerances can be maintained and duplicated---especially when compared to the former two methods.

All three methods are feasible. For any of them, detailed techniques would need to be developed. Throughout the etch process, for example, electrical monitoring of the resultant current-voltage characteristic would be necessary. The process would be stopped when the desired characteristic is achieved.

The chip removed is that of the diode designed and shown to obey the $\frac{1}{V^2}$ law. The (2.75,1) coordinate was chosen for convenience. In actual fabrication some other coordinate may prove better. It is suspected that the removal of a chip constituting the whole original upper surface of the pinch-off diode is one to be strongly considered.

The last stage in the fabrication is canning the device. A standard transistor can would suffice. Canning is necessary to remove light from the device and to insulate the device from changes in ambient humidity. Potting, pressure sealing in dry gas or evacuation is acceptable.

No devices of the design speculated upon were fabricated. Precision

equipment for slicing, lapping, polishing, photo-lithographing, dicing, etching and canning is not available at Iowa State University.

SUMMARY

In this dissertation a method for generating particular current-voltage characteristics for semiconductor pinch-off diodes has been described. It has been shown which material parameters are salient in the design of a diode. The material parameters have been shown to link the physical size of the diode to the voltage level at which the diode will be operated.

The geometrical configuration has been shown to affect the current-voltage relationship. A design of a representative current-voltage characteristic, $I = K \sqrt{\frac{1}{V}}$, has been effected by means of an iterative approach. The current-voltage characteristic has been developed by computing the resistance of the diode studied for a particular drain voltage.

The resistance presented has been calculated by means of a determination utilizing curvilinear squares. The squares have been produced by determining the potential distribution across the diode by means of a solution to Laplace's equation. The solution has been effected by a computer solution using finite-difference equations.

The device developed is predicted to have a cut-off frequency in the order of 10×10^6 cycles per second. Proper design for frequency improvement, if that be the criteria, should be able to raise the cut-off frequency by a factor of two to three.

In many cases 25×10^6 cycles per second is entirely adequate. In others it is not. The reason for the rather low cut-off frequency is that the geometry is a more or less planar one. If higher frequencies were necessary, this requirement would have to be a design criteria. In all probability, cut-off frequencies could be improved by going to non-planar

devices.

A proposed method of fabrication is presented. Provided that sufficient precise fabrication equipment is available, this device can be rather easily produced.

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APPENDIX A

The x-y plane cross-section of Shockley's field-effect transistor shown in Figure 1 and described mathematically before pinch-off by equation 1 is shown in Figure 23. The physical distance between the two p-type regions is a . The distance between the two depletion layer boundaries is b . The distance b is the dimension which dictates the conducting cross-section of the diode. Choice of coordinates dictates that the distances to the centerline of the diode are $\frac{a}{2}$ and $\frac{b}{2}$. The length of the gate diode L is shown.

As in all diodes described, the body of the diode is n-type semiconductor, and the alloyed or diffused material is p-type. The doping levels of the two materials are arranged such that $N_a \gg N_d$.

In order to find the depletion layer penetration as a function of the applied voltage to the drain, Poisson's equation in one dimension will be solved. The boundary conditions are that $E_y = 0$ at $y = \frac{b}{2}$ and that $V_y = 0$ at $y = \frac{a}{2}$. These are consistent with the boundary conditions in the section on Poisson's equations relative to finding the applied voltage-depletion layer depth relation.

Integrating

$$\frac{\partial^2 V}{\partial y^2} = -\frac{\rho}{\epsilon} = -\frac{q N_d}{\epsilon} \quad (67)$$

once and evaluating the constant of integration gives

$$\frac{\partial V}{\partial y} = E_y = -\frac{q N_d}{\epsilon} \left(y - \frac{b}{2} \right) \quad (68)$$

Integrating again and evaluating the constant results in the voltage V_y .

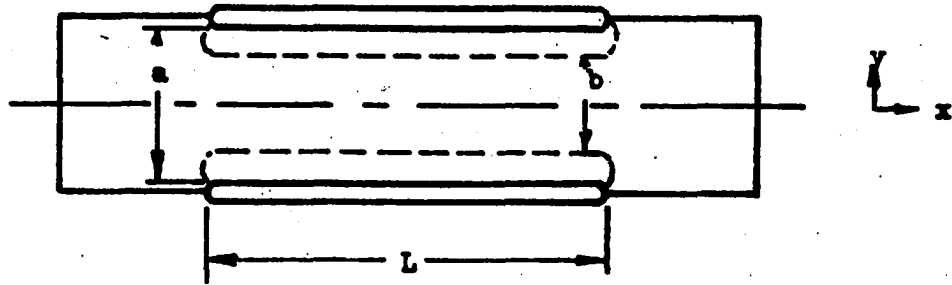


Figure 23. The x-y plane cross-section of Schockley's field-effect transistor

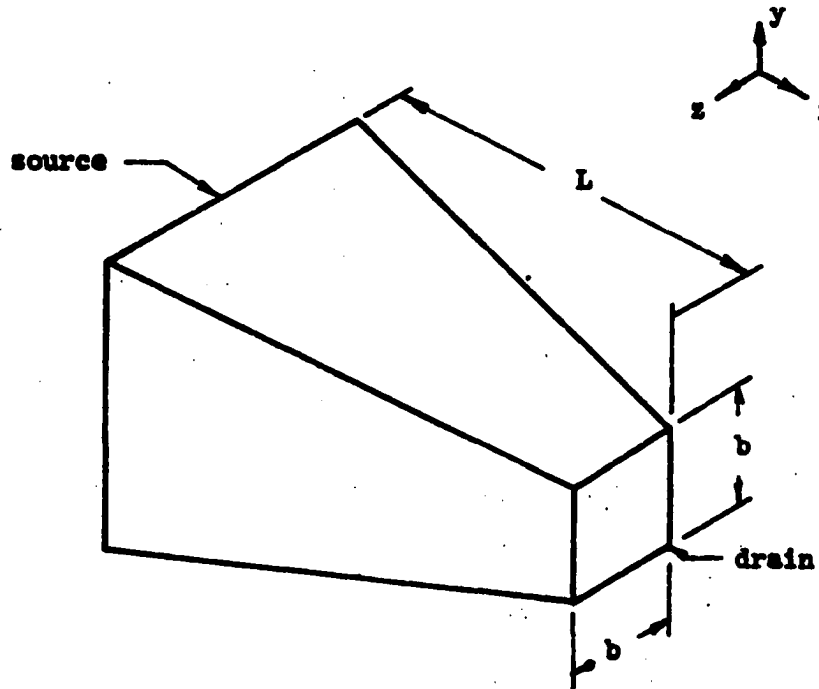


Figure 24. The conducting channel for Schockley's field-effect transistor

$$V_y = - \frac{q N_d}{2\epsilon} \left[\left(y - \frac{b}{2} \right)^2 - \left(\frac{a}{2} - \frac{b}{2} \right)^2 \right] . \quad (69)$$

In order to obtain the voltage existing across the junction it is necessary to set $y = \frac{b}{2}$. Performing this operation and slightly reorganizing gives

$$V = \frac{q N_d}{8\epsilon} a^2 \left(1 - \frac{b}{a} \right)^2 . \quad (70)$$

It is seen that, when a certain voltage is applied to the drain, b will become zero. The conducting channel goes to zero and is pinched-off. The value of voltage necessary to pinch-off the diode is V_o .

$$V_o = \frac{q N_d}{8\epsilon} a^2 . \quad (71)$$

Equation 70 may be rewritten as

$$V = V_o \left(1 - \frac{a}{b} \right)^2 . \quad (72)$$

Solving for b in terms of the applied voltage to the junction results in

$$b = a \left[1 - \left(\frac{V}{V_o} \right)^{\frac{1}{2}} \right] . \quad (73)$$

Figure 24 shows the conducting channel of the field-effect transistor. No new terms have been introduced.

Ohm's law in differential form is

$$I dr = dV . \quad (74)$$

The expression for dr is

$$dr = \frac{\rho dx}{A} = \frac{\rho dx}{b^2} . \quad (75)$$

A is the conducting cross-section normal to the current flow.

To obtain the current-voltage characteristic, equations 73, 74 and 75 are combined, regrouped and integrated over the ranges shown. V_D is momentarily the notation for the drain voltage.

$$\int_0^L I \, dx = \frac{a^2}{\rho} \int_0^{V_D} \left[1 - \left(\frac{V}{V_0} \right)^2 \right]^2 \, dV \quad (76)$$

Equation 77 shows the result of the integration.

$$I = \frac{a^2}{\rho L} \left[V_D - \frac{4}{3} \frac{V_D^{\frac{3}{2}}}{V_0^{\frac{1}{2}}} + \frac{1}{2} \frac{V_D^2}{V_0} \right] \quad (77)$$

Since it does not matter what symbol describes the drain voltage, V_D may be changed to V in order to form equation 1.

This solution is effected by considering the gate voltage to be zero relative to the source. If a gate bias is supplied, it does nothing more than increase the amount of voltage applied across the p-n gate diode; consequently, one may directly write down the current-voltage relationship for the field-effect transistor for non-zero gate voltages.

$$I = \frac{a^2}{\rho L} \left[(V - V_g) - \frac{4}{3} \frac{(V - V_g)^{\frac{3}{2}}}{V_0^{\frac{1}{2}}} + \frac{1}{2} \frac{(V - V_g)^2}{V_0} \right] \quad (78)$$

V_g is the gate voltage.

APPENDIX B

If a pinch-off diode is fabricated similar to that of Figure 3 except that p-n junctions are formed on both the upper and lower surfaces, the solution for V as a function of b and the solution for V_0 are identical to equations 71 and 73. The only change from Schockley's solution is that the conducting channel is no longer square in cross-section but rectangular with height b and width z_0 .

Equation 79 is

$$dr = \frac{\rho \, dx}{A} = \frac{\rho \, dx}{z_0 b} \quad . \quad (79)$$

The integral expression is

$$\int_0^L I \, dx = \frac{z_0 a}{\rho} \int_0^{V_D} \left[1 - \left(\frac{V}{V_0} \right)^{\frac{1}{2}} \right] dV \quad . \quad (80)$$

Evaluating and changing variables as in the Schockley description results in

$$I = \frac{z_0 a V_0}{\rho L} \left\{ \frac{V}{V_0} \left[1 - \frac{2}{3} \left(\frac{V}{V_0} \right)^{\frac{1}{2}} \right] \right\} \quad . \quad (81)$$

If this device were to be used as a field-effect transistor, an equation analogous to equation 78 could be developed.

Equation 81 is identical to equation 55 except for the evaluation for V_0 . In equation 81, V_0 is evaluated by equation 71. In equation 55, V_0 is evaluated by equation 13.

Equation 71 and equation 13 differ only by a constant of four. This number results from the fact that the thickness of the one-side diffused

diode has a height of a as does the two-side diffused diode. The factor a enters into the equation as a^2 ; hence the factor of four is introduced.

APPENDIX C

Although more of a windfall than a design, it is possible to form a device incorporating Schockley's device and the rectangular cross-section diode which will obey the equation

$$I_1 = K_1 V^2 \quad . \quad (82)$$

In order to keep the parameters separated, equation 81 is rewritten using the subscript 2.

$$I_2 = \frac{z_o a_2}{\rho_2 L_2} V \left[1 - \frac{2}{3} \left(\frac{V}{V_{o2}} \right)^2 \right]^{\frac{1}{2}} \quad . \quad (83)$$

If the difference of equation 77 and 83 can be formed,

$$\begin{aligned} I_1 &= I - I_2 = \\ &= \frac{a^2 V}{\rho L} \left[1 - \frac{4}{3} \left(\frac{V}{V_o} \right)^2 + \frac{1}{2} \frac{V}{V_o} \right] \\ &\quad - \frac{z_o a_2}{\rho_2 L_2} V \left[1 - \frac{2}{3} \left(\frac{V}{V_{o2}} \right)^2 \right]^{\frac{1}{2}} \quad . \end{aligned} \quad (84)$$

By imposing the restriction on the device parameters that

$$\frac{4}{3} \frac{a^2}{\rho L} V_o^{\frac{1}{2}} = \frac{2}{3} \frac{z_o a_2}{\rho_2 L_2} V_{o2}^{\frac{1}{2}} \quad , \quad (85)$$

the terms involving $V^{\frac{3}{2}}$ will cancel out.

The result after some regrouping is

$$I_1 = \frac{a^2}{\rho L} \left\{ \left[1 - 2 \left(\frac{V}{V_o} \right)^2 \right]^{\frac{1}{2}} V + \frac{1}{2} \frac{V^2}{V_o} \right\} \quad . \quad (86)$$

If a further restriction is imposed on the pinch-off voltages such that

$$\frac{V_{o2}}{V_o} = \frac{1}{4} , \quad (87)$$

the terms involving V may be removed.

It is also possible that the term involving V in equation 86 is negative. In this event the term involving V may be removed by shunting the device by a fixed conductance equal in size to the magnitude of the coefficient of V . In this event, the criteria of equation 87 need not be effected.

A circuit which will perform the differencing function is shown in Figure 25. The current I_{in} is made proportional to the voltage to be squared. R_a and R_b provide base bias. R_c and R_e are nearly equal except for any β considerations. They are chosen nearly equal in order that as the emitter current increases, the emitter voltage will increase as much as the collector voltage decreases.

The transistor load comprised of the two diodes, R_d , the ammeter and the Zener diode must present an impedance large with respect to R_c plus R_e . This condition is necessary in order that the transistor not be loaded appreciably and that the emitter and collector voltage be controlled by the IR drops of R_c and R_e .

The Zener diode is chosen to have a voltage equal to the midway between the quiescent collector voltage and emitter voltage. At that point the Shockley diode will have as much voltage as the other diode. The polarities will be different.

This whole circuit lends itself to miniaturization. All the elements except the two pinch-off diodes could be fabricated on the same piece of

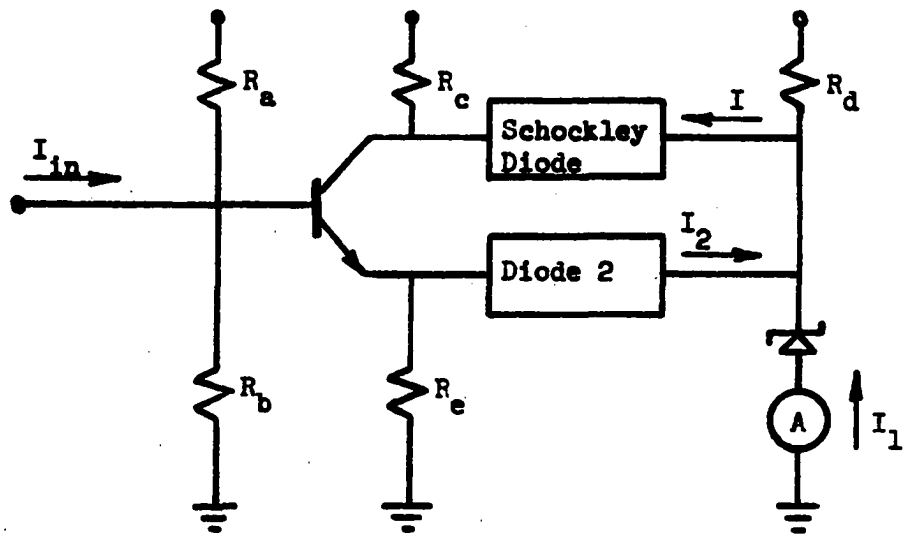


Figure 25. Circuit for current differencing

semiconductor. With a little experimentation, it is likely that even the two pinch-off diodes or similar ones could be incorporated into the semiconductor slice.